Using the MSO-19 with the Electronics Learning Lab

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This series of labs is designed to demonstrate the use of the MSO-19 Oscilloscope/Logic Analyzer/Pattern Generator in an educational environment. The lessons build on the Radio Shack Electronics Learning Lab. They provide insight into the inner workings of the circuit with the use of high performance test and measurement equipment. It is a primer on the use of Oscilloscopes, Logic Analyzers and Pattern Generators (digital word generators).

The lessons go beyond switches and the simple flashing lights of the original labs. The waveforms are displayed on an Oscilloscope and Logic Analyzer. The Pattern Generator provides a repeatable data stream to the circuit without the need of toggling switches.

The powerful features and high-performance of the MSO-19 provide a great platform to teach and easily demonstrate advanced topics such as the affects of propagation delay, slew rate, hysteresis, setup times, etc…

Preconfigured settings files are provided to make setup and lesson plans easy. More sophisticated students can setup the instrument themselves. The windows based software simplifies lab report creation.

Table on contents

555 Timer

Reference: Radio Shack Electronics Learning Lab (28-280) Workbook 1, page 15.

Tools: Radio Shack Electronics Learning Lab
Link Instruments MSO-19 Oscilloscope/Logic Analyzer/Pattern Generator

Overview: This lab is a supplement to the Radio Shack Electronics Learning Lab. It provides additional insight into the circuit with the use of an Oscilloscope.

The venerable 555 Timer IC is a chip that every budding Electrical Engineer needs to be familiar with as a rite of passage. The 555 will be wired in an astable configuration. We will start out by creating a simple circuit that uses the 555 Timer IC to flash a LED. You will use the MSO-19 Oscilloscope to view the inner workings of the circuit. The Oscilloscope will be used to probe various test points and give you more insight into the workings of the circuit than you would get with the LEDS provided in the original lab.

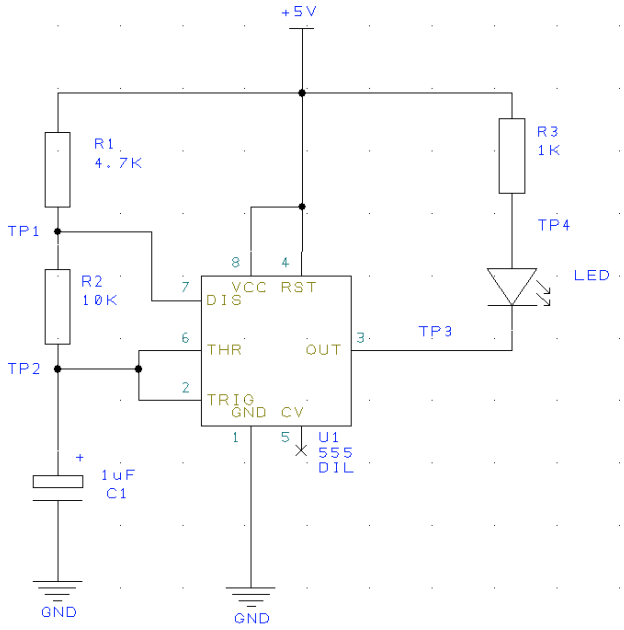


Figure 1:

This is the circuit from page 15 with C1 changed from 10uF to 1uF. This will make the LED flash faster.

Below are the Test Points waveforms captured on the MSO-19's oscilloscope.

TP1

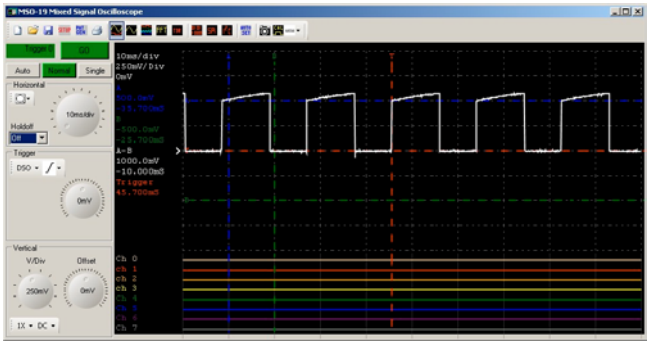


Figure 2: (MSO-19 File: TP1.MSD)

This is the Discharge pin. One can see the charging ramp as the voltage builds up and the discharge period.

TP3

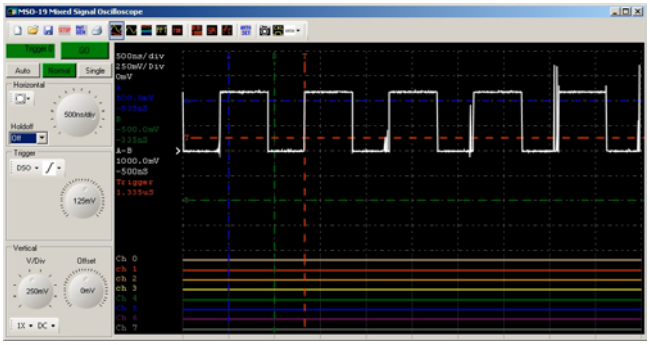


Figure 3: (MSO-19 File: TP3.MSD)

This is the Output pin. It turns on the LED by pulling the output to GND. Notice the glitches at the rising edge.

TP2

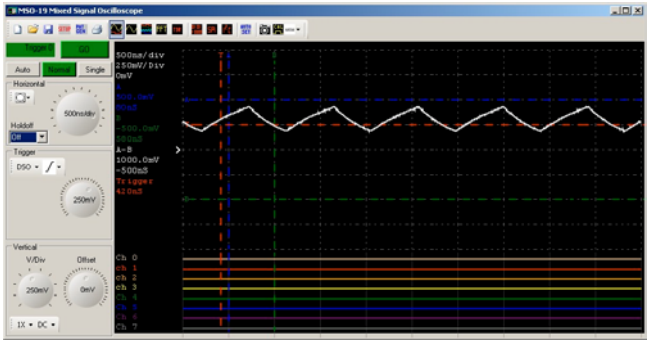


Figure 4: (MSO-19 File: TP2.MSD)

This is the voltage at the capacitor C1. One can see the charging and discharging ramps.

TP4

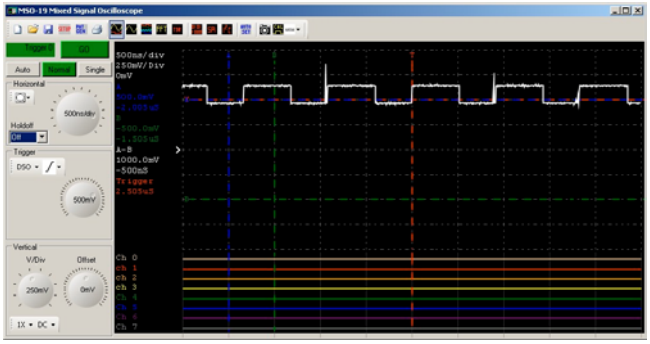
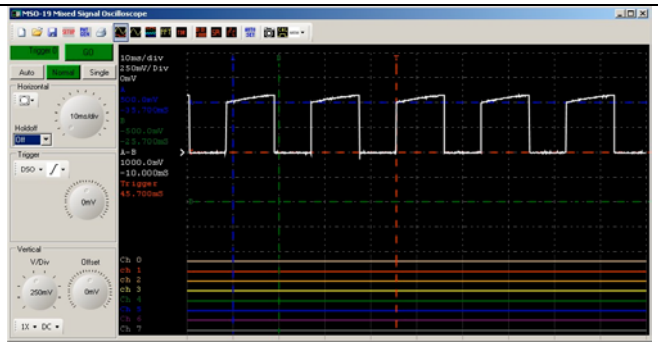
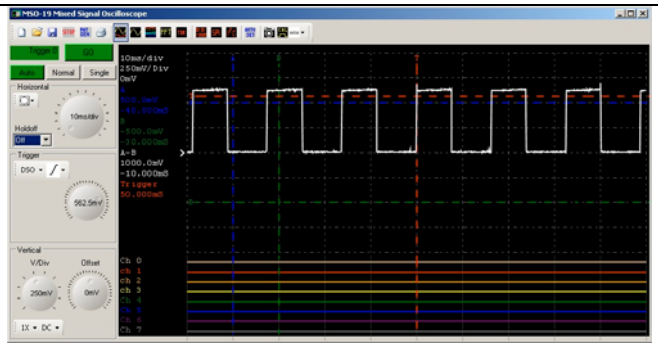
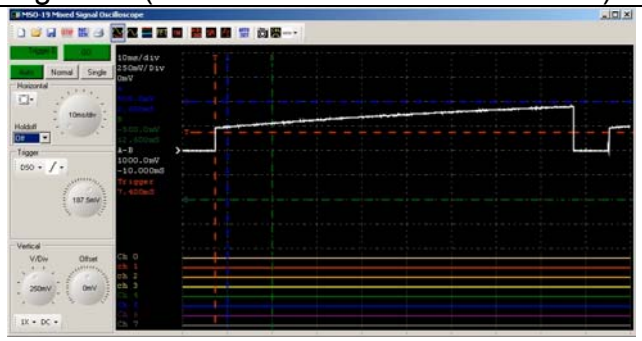
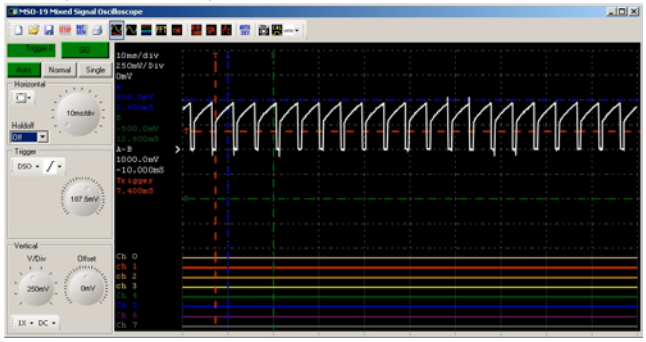
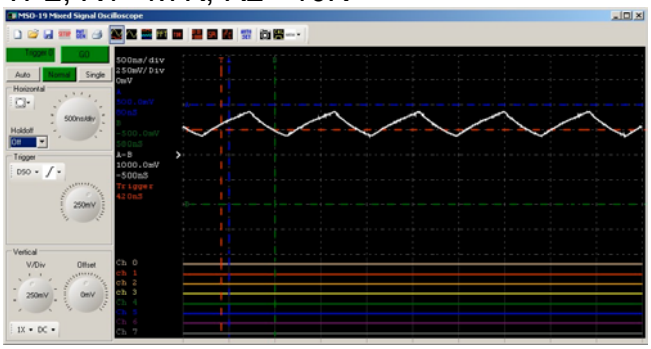
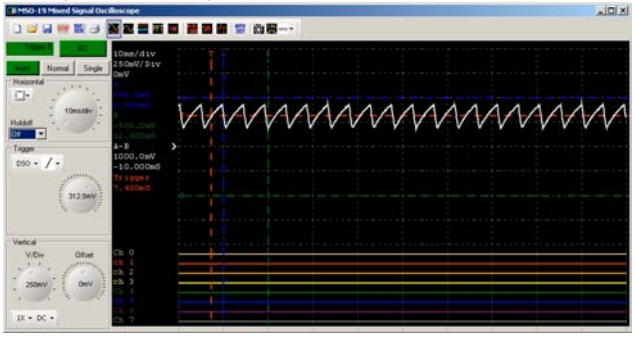
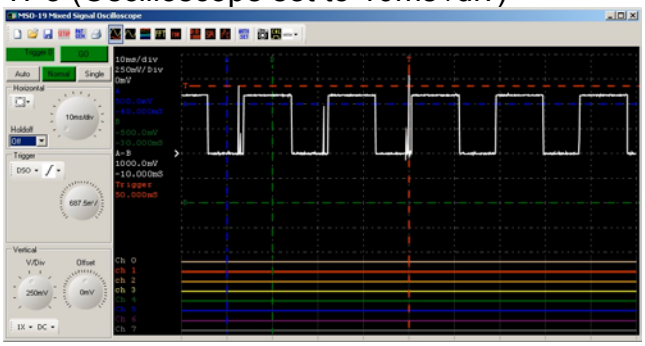
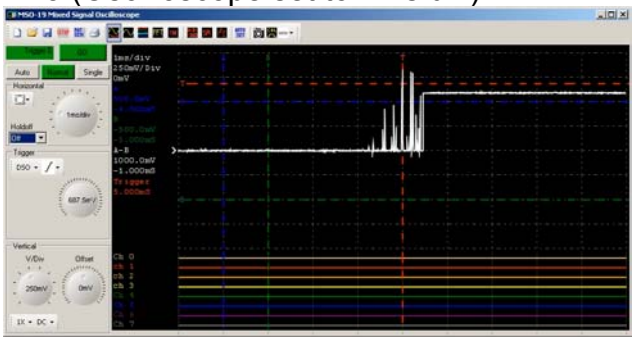
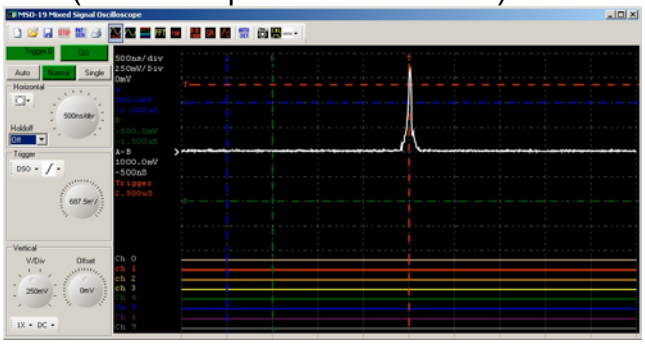


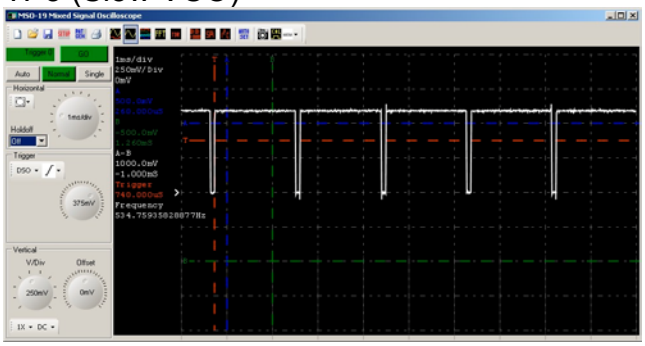
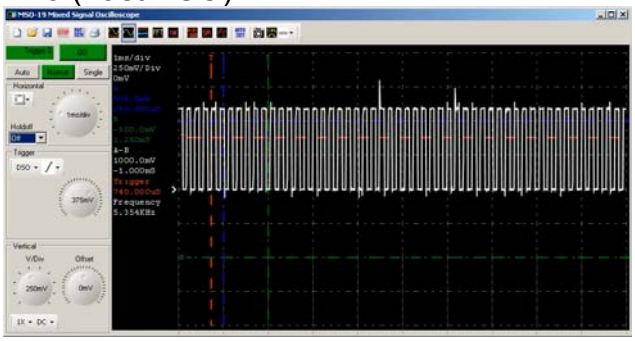
Figure 5: (MSO-19 File: TP4.MSD)

Notice the voltage drop on R3 when the LED is turned ON.

TP1	
The frequency on the 555 is defined by 1 / (T1(charge time) + T2(discharge time)) The charge time is defined as T1 = 0.693 x (R1+R2) x C1 The discharge time is defined as T2 = 0.693 x (R2) x C1 T1 is the high part of the square wave. T2 is the low part of the square wave.	 Figure 6: (MSO-19 File: TP1.MSD)
By changing R1 resistance we change the charge rate and frequency. If we change R1 from 4.7K ohm to 470 ohm the charge rate speeds up. Note: the difference in the ramp shape on the top of the square wave. The frequency has increased as demonstrated by the increased number of pulses.	 Figure 7: (MSO-19 File: TP1 R1 470.MSD)
Increasing R1 has the opposite effect. As we see in the example of changing R1 to 100K. Note: the discharge time stayed constant.	 Figure 8: (MSO-19 File: TP1 R1 100K.MSD)
If we change the discharge resister R2 from 10K to 1K the discharge time is reduced. The low time is now 1/10 of the duration. The change to the high part of the waveform is not as drastic.	TP1, R1=4.7K, R2= 1K  Figure 9: (MSO-19 File: TP1 R2 1K.MSD)

TP2	
View of capacitor C1's charge and discharge waveform.	TP2, R1=4.7K, R2= 10K  Figure 10: (MSO-19 File: TP2.MSD)
Notice the sharp discharge ramp that was the result of changing R2 from 10K to 1K.	TP2, R1=4.7K, R2= 1K  Figure 11: (MSO-19 File: TP2 R2 1K.MSD)

TP3	
An interesting side note. On the TP3 plot we see some noise on the rising edge. Since the MSO-19 can sample at 200Msa/S, we can speed up our timebase and zoom in on the glitches. The glitches are generated by the threshold circuit inside the 555 IC. It is due to the slow rise time.	TP3 (Oscilloscope set to 10ms /div)  Figure 12: (MSO-19 File: TP3 Glitch 1.MSD)
	TP3 (Oscilloscope set to 1ms/div)  Figure 13: (MSO-19 File: TP3 Glitch 3.MSD)
	TP3 (Oscilloscope set to 500ns/div)  Figure 14: (MSO-19 File: TP3 Glitch 2.MSD)

VCO	
Pin 5 on the 555 is the voltage control pin. By changing the input voltage on pin 5 we can further alter the frequency. The variable resister, circuit diagram on page 89 of Radio Shack Workbook 1, affects this input voltage. The two oscilloscope pictures to the right show the affect of turning the variable resistor.	TP3 (Slow VCO)  Diagram 15 (VCO slow.MSD)
	TP3 (Fast VCO)  Diagram 16 (VCO fast.MSD)

Operational Amplifier

Reference: Radio Shack Electronics Learning Lab (28-280) Workbook 1, page 72.

Tools: Radio Shack Electronics Learning Lab
TL272 Dual Amplifier
Link Instruments MSO-19 Oscilloscope/Logic Analyzer/Pattern Generator

Overview: This lab is a supplement to the Radio Shack Electronics Learning Lab. It is also a demonstration of the MSO-19 Oscilloscope and Function Generator.
In today's world of high-speed digital electronics the importance of analog circuits are often overlooked. Operational Amplifiers (OP Amps) are the fundamental building blocks of modern analog electronic designs. Two of the most popular topologies are Inverting and Non-Inverting amplifiers. In this exercise we will build a non-inverting amplifier with a gain of two using the TL272 IC.

The MSO-19 Function Generator will output a 1 bit pulse train which can be filtered with a low-pass filter to generate a sine wave output. This is the theory behind 1 bit DAC technology found in CD players.

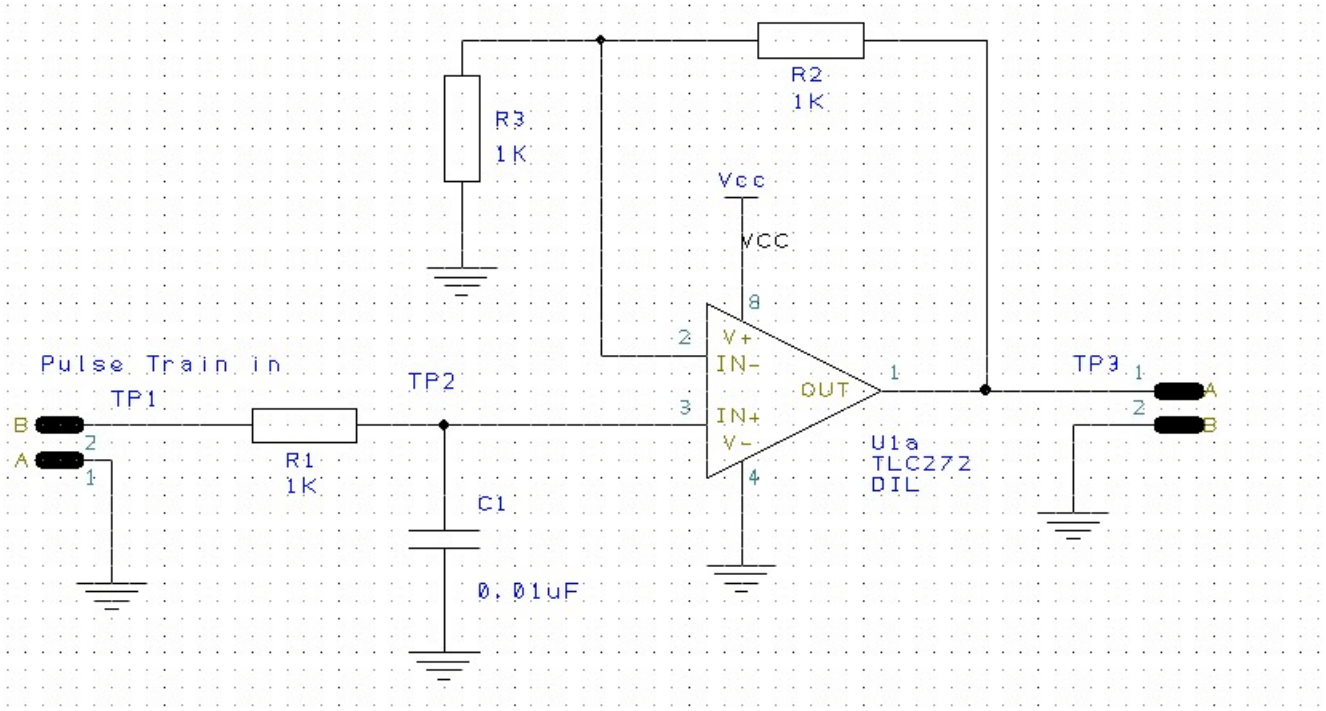
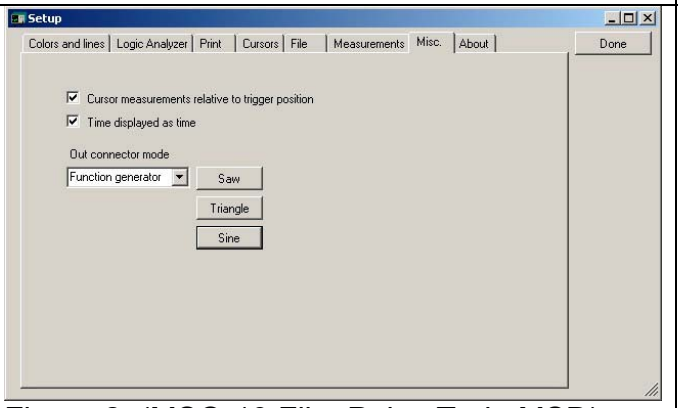
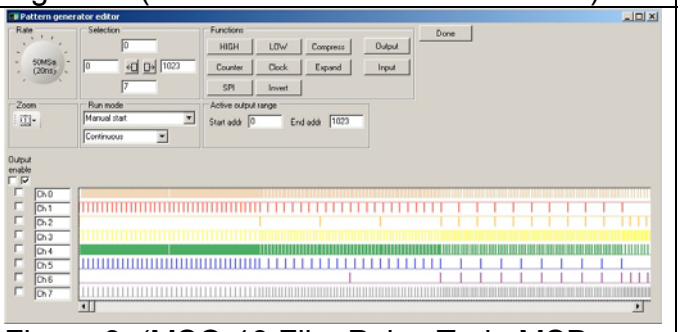
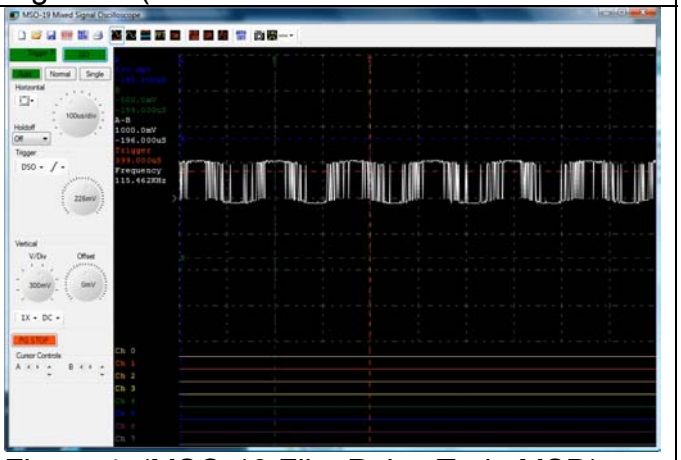
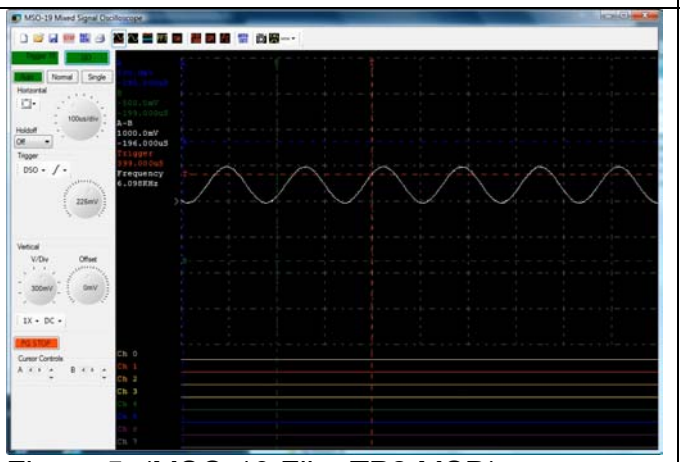
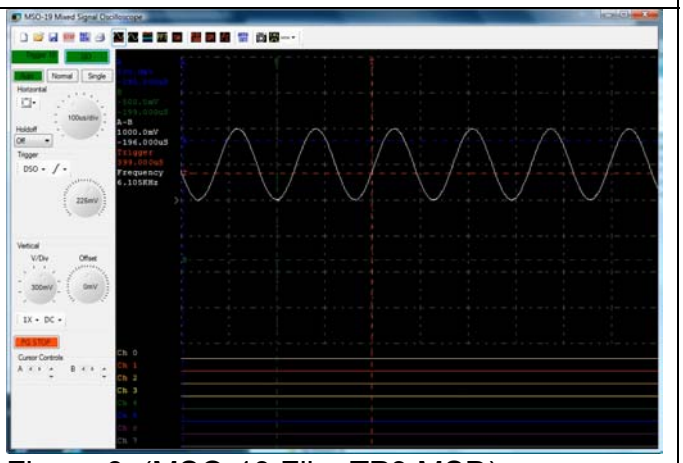
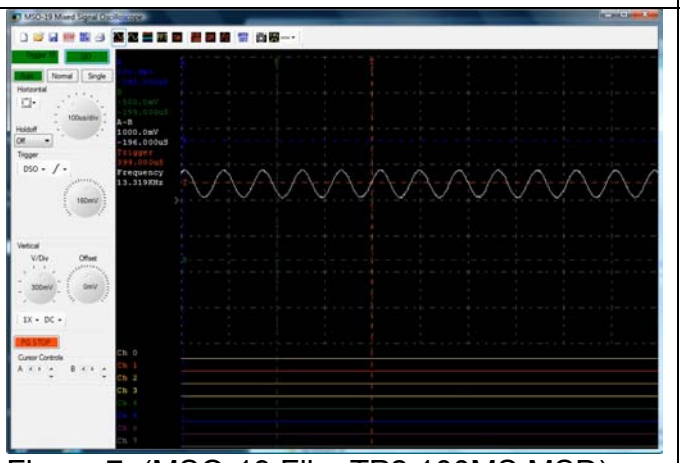


Figure 1:

TP1 (output of MSO-19)	
Configure the MSO-19's function generator to create a sine wave. Select Setup->Misc->Function Generator And click on **Sine.** This will create a 1 bit DAC data stream that will be output from the MSO-19 BNC connector. By filtering this pulse train with a low-pass filter we can remove the high-frequency component and generate a sine wave.	 Figure 2: (MSO-19 File: Pulse Train.MSD)
This sets up the PG buffer with a pulse train pattern for Sine Wave. Select 50Msa. This will create a sine of 6.1Khz. Selecting other rates will create different output frequencies.	 Figure 3: (MSO-19 File: Pulse Train.MSD
Measuring from TP1 we see the pulse train output.	 Figure 4: (MSO-19 File: Pulse Train.MSD)

TP2 (Output of low-pass filter)	
TP2 shows the output to the low-pass. You will see a clean sine wave. This sine wave is the input for our amplifier experiment.	 Figure 5: (MSO-19 File: TP2.MSD)

TP3 (output of amplifier)	
With a gain of 2, we can see that the output sine wave is twice the size of the input sine wave.	 Figure 6: (MSO-19 File: TP3.MSD)

TP2 (Output of low-pass filter)	
Adjusting the PG sample rate of Figure 3 will affect the frequency of the signal seen at TP2. This is a picture of the output if sped up the sine wave by increasing the Pattern Generator rate to 100Msa.	 Figure 7: (MSO-19 File: TP2 100MS.MSD)

CMOS Oscillator

Reference: Radio Shack Electronics Learning Lab (28-280) Workbook 2, page 24.

Tools: Radio Shack Electronics Learning Lab
MC14001IC
Link Instruments MSO-19 Oscilloscope/Logic Analyzer/Pattern Generator

Overview: This lab is a supplement to the Radio Shack Electronics Learning Lab (28-280) Workbook 2, page 24. It is also a demonstration of the MSO-19 Oscilloscope and Logic Analyzer.
NAND and NOR gates can be use to create a simple oscillator. In the exercise, we will build an oscillator out of two NOR gates and explore the pins. The circuit will be based on Radio Shack's Electronics Learning Lab (28-280) and the MC14001 that comes in the kit. Refer to the "Digital Logic Projects" Workbook 2, page 24 for more details. Component value of C1 will change from 10uF to 0.1uF, to crank the frequency up a few notches.

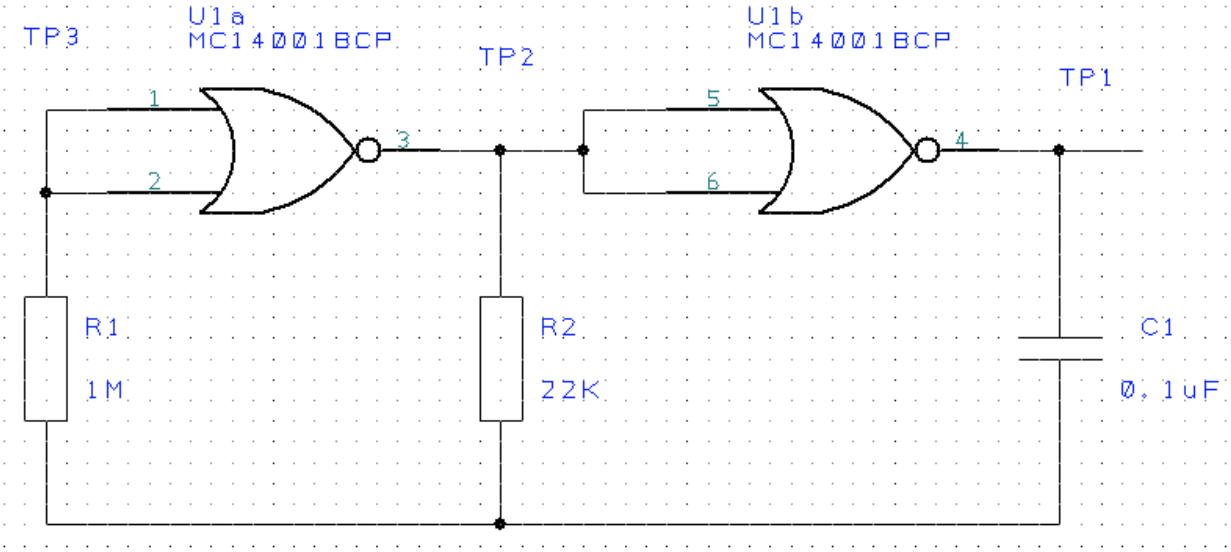
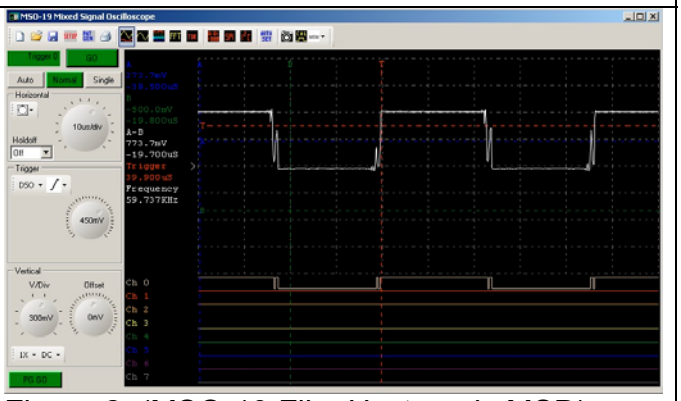
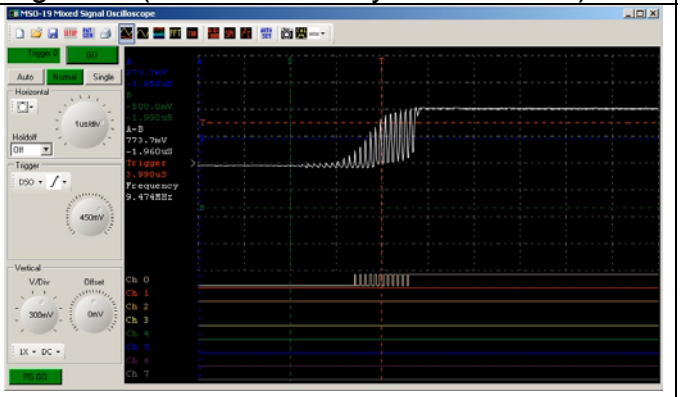
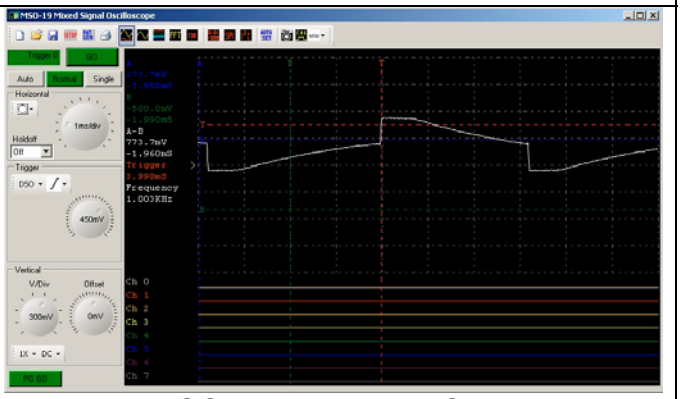
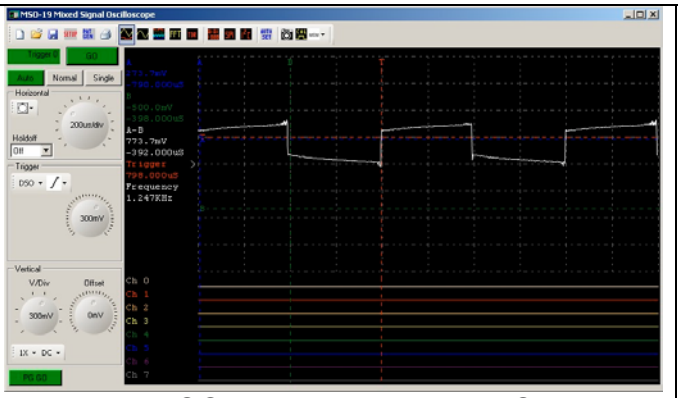


Figure 1:

TP1	
The Oscilloscope probe and Logic Analyzer channel 0 are both connected to TP1. The Oscilloscope input can display the analog waveform and the voltage level at any point measured. The Logic Analyzer only displays the “Logic High” and “Logic Low” signal. Notice the noise at the rising and falling edge of each pulse.	 Figure 2: (MSO-19 File: Hysteresis.MSD)
By increasing the sample rate we can see greater edge detail. Notice how the Oscilloscope trace shows a gradual voltage rise and the Logic Analyzer can only show the high or low state.	 Figure 3: (MSO-19 File: Hysteresis closeup.MSD)
TP3	
The noise seen in Figure 3 is caused by the slow rise time at TP3. This causes the NOR gate to see multiple transitions at its logic threshold.	 Figure 4: (MSO-19 File: TP3.MSD)

To alter the frequency of the oscillator, we can change the value of R2. For example, changing R2 from 22K ohm to 2.2K ohm will increase the oscillation frequency.	 Figure 5: (MSO-19 File: TP1_222.MSD)

One shot

Reference: Radio Shack Electronics Learning Lab (28-280) Workbook 2, page 25.

Tools: Radio Shack Electronics Learning Lab
MC14001IC
Link Instruments MSO-19 Oscilloscope/Logic Analyzer/Pattern Generator

Overview: This lab is a supplement to the Radio Shack Electronics Learning Lab. It is also a demonstration of the MSO-19 Oscilloscope, Logic Analyzer and Pattern Generator.

A “One shot” circuit is used to stretch the width of a pulse. We will build a circuit based on Radio Shack’s Electronics Learning Lab (28-280) and the MC14001 that comes in that kit.

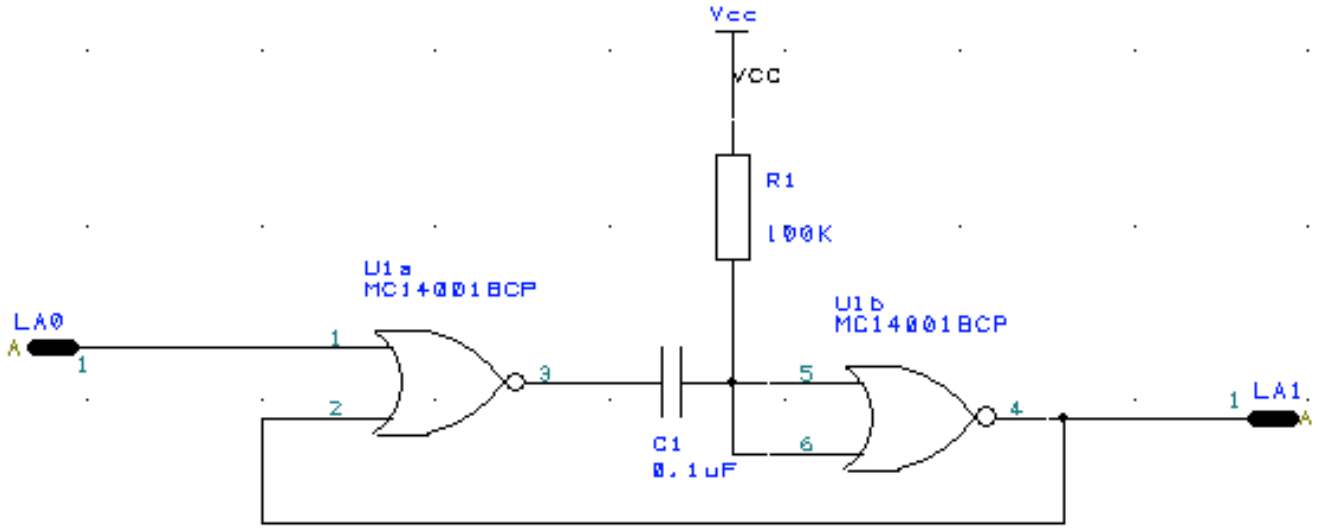
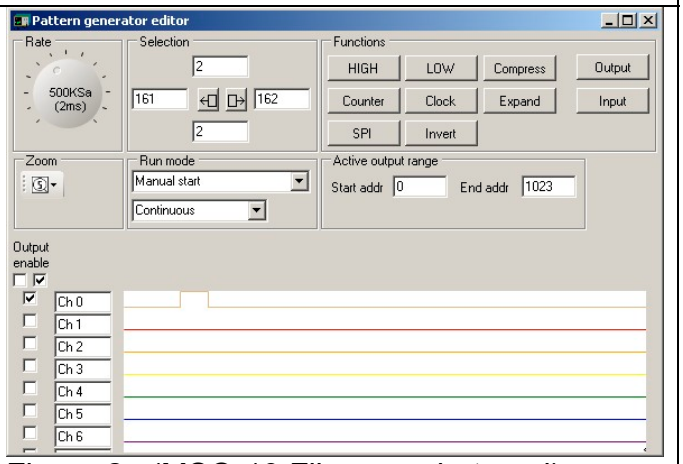
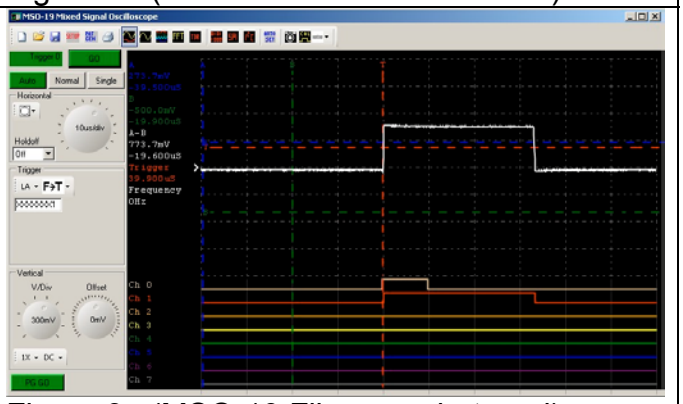
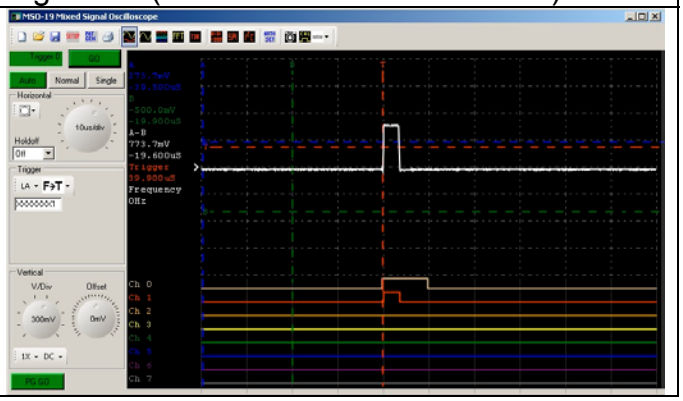


Figure 1:
The component value of C1was set to 0.1uF and R1 was set to 100K ohm to speed up the circuit.

The Pulse width of our one shot is defined by the RC constant of R1 and C1. We will use the MSO-19 Pattern Generator to create a pulse for the “One shot” to stretch. We will use the MSO-19 Logic Analyzer to capture the original pulse and the stretched pulse of the “One shot”.	
Notice the single pulse on channel 0. Please refer to the MSO-19 manual for more information on creating a pulse.	 Figure 2: (MSO-19 File: one shot.msd)
The Pattern Generator output can be seen on Logic Analyzer channel 0. The Oscilloscope channel and Logic Analyzer channel 1 demonstrate the stretched signal from the “One shot”. Notice that our 10uS pulse (Ch0) is now stretched to 33uS wide (Ch1).	 Figure 3: (MSO-19 File: one shot.msd)
It is also possible to create a shorter pulse than our original pulse. Changing R1 from 100K to 10K, we get a smaller time constant, therefore a shorter pulse. The original 10uS pulse did not change, but the output of the “One shot” did.	

1 bit adder

Reference: Radio Shack Electronics Learning Lab (28-280) Workbook 2, page 54.

Tools: Radio Shack Electronics Learning Lab
CD4011 and CD4070 ICs
Link Instruments MSO-19 Oscilloscope/Logic Analyzer/Pattern Generator

Overview: This lab is a supplement to the Radio Shack Electronics Learning Lab. It is also a demonstration of the MSO-19 Oscilloscope, Logic Analyzer and Pattern Generator.

One of the key functions of a modern digital computer is the ability to add. Subtraction, multiplication and division all derive from the add function. A Binary Adder is the basic building block from which larger adders are created. In this example we will build a Binary Full Adder.

The MSO-19 Pattern Generator output pins will replace the two input switches of the original lab. The operation of the circuit will be monitored on the Logic Analyzer pins of the MSO-19.

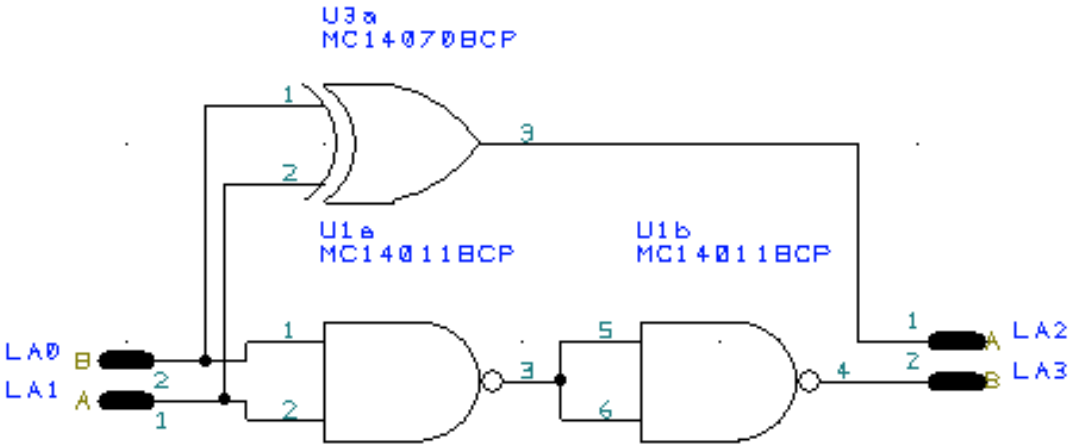


Figure 1:

The Pattern Generator Channels 0 and 1 will simulate all the possible switch combinations, by generating the input conditions as a 2 bit counter.

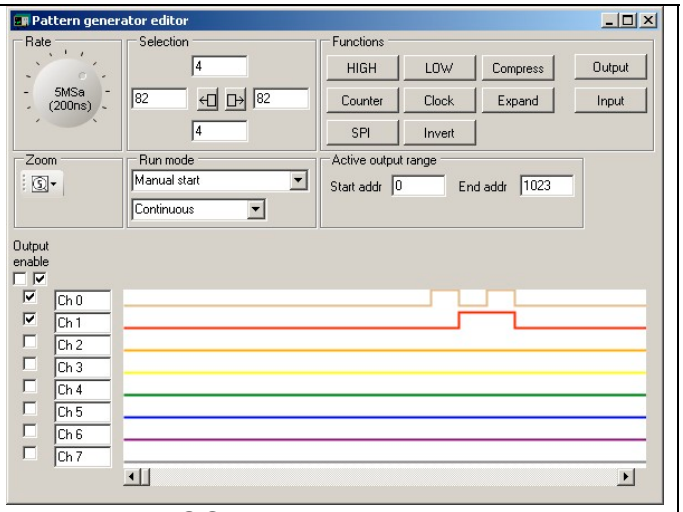


Figure 2: (MSO-19 File: Adder.msd)

Logic Analyzer channels 0 and 1 show the input to the adder.
Logic Analyzer channels 2 and 3 show the output of the adder.

As expected, the output matches the truth table on page 54. An interesting side note is that the output lags the input by 180ns. This is the propagation delay of this circuit through two ICs and wires. This will limit the operating frequency of this circuit to about 5.55Mhz.

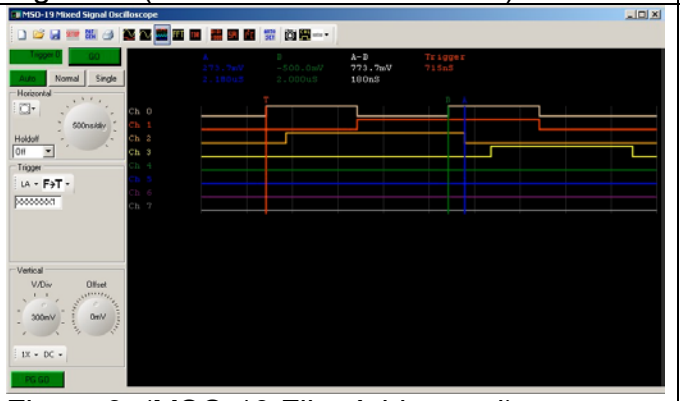


Figure 3: (MSO-19 File: Adder.msd)

4 input NAND gate

Reference: Radio Shack Electronics Learning Lab (28-280) Workbook 2, page 44.

Tools: Radio Shack Electronics Learning Lab
CD4011 IC
Link Instruments MSO-19 Oscilloscope/Logic Analyzer/Pattern Generator

Overview: This lab is a supplement to the Radio Shack Electronics Learning Lab. It is also a demonstration of the MSO-19 Logic Analyzer and Pattern Generator.

Other than the inverter, most simple logic functions involve two inputs and one output. These functions can be AND, OR, XOR and their complements of NAND, NOR, XNOR. Complex functions can be created by mixing and matching the above mentioned building blocks into larger circuits. In this example, we will build a 4 input NAND gate out of five 2 input NAND gates.

The MSO-19 Pattern Generator output pins will replace the four input switches of the original lab. The operation of the circuit will be monitored on the Logic Analyzer pins of the MSO-19.

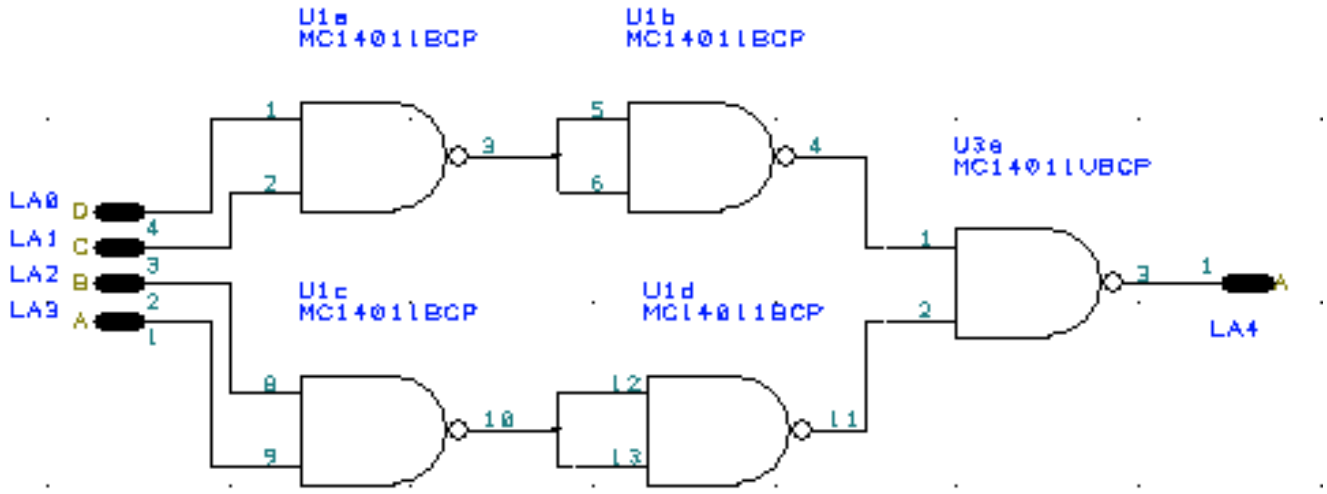
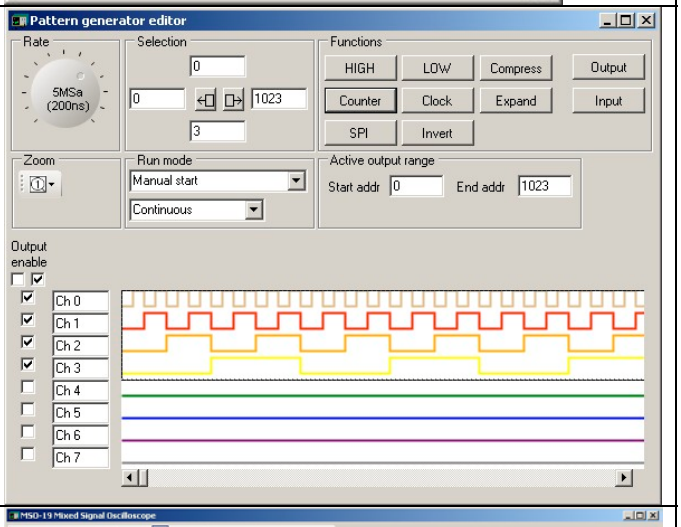
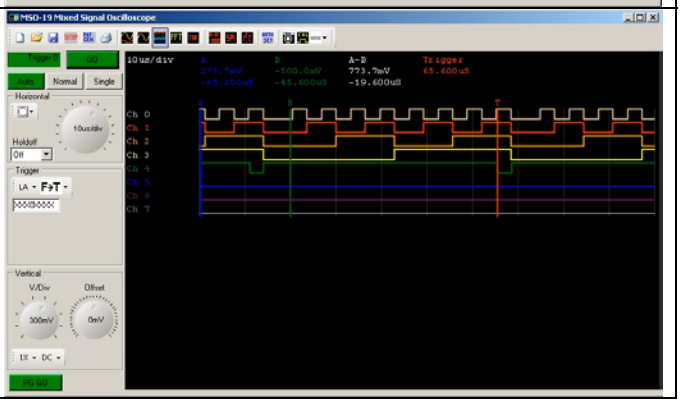


Figure 1:

In the original lab you used 4 input switches to stimulate the 16 possible inputs to the circuit. In this version we will use the MSO-19 Pattern Generator to generate those 16 combinations. Start the MSO-19 Pattern Generator editor and select counter. We set start to 0 and stop to 15 to give us 16 possible values.	
The Pattern Generator output is now configured to count from 0 though 15 (16 possible values).	
Logic Analyzer channels 0, 1, 2 and 3 show the 4 inputs to the NAND gate. Logic Analyzer channel 4 shows the output of the NAND. The output matches the truth table on page 45 of the workbook.	

4 input comparator

Reference: Radio Shack Electronics Learning Lab (28-280) Workbook 2, page 56.

Tools: Radio Shack Electronics Learning Lab
CD4070, CD4049 and ICD4011 ICs
Link Instruments MSO-19 Oscilloscope/Logic Analyzer/Pattern Generator

Overview: This lab is a supplement to the Radio Shack Electronics Learning Lab. It is also a demonstration of the MSO-19 Oscilloscope, Logic Analyzer and Pattern Generator.

Digital comparators are important building blocks in digital computers. They perform the all important IF function. In the simplest form, a comparator is just a XOR gate. Multi-bit comparators are constructed by combining the outputs of multiple XOR gates.

In this exercise we will use CD4070, CD4049 and ICD4011 ICs to form a 4 bit comparator.

The MSO-19's Pattern Generator will be used to cycle through the 16 possible states. This is accomplished by creating a 4 bit counter. The original lab used wires to encode the 4 mystery bits. We will be using the Pattern Generator for that also.

We will monitor the output of the circuit with the Oscilloscope and Logic Analyzer channels.

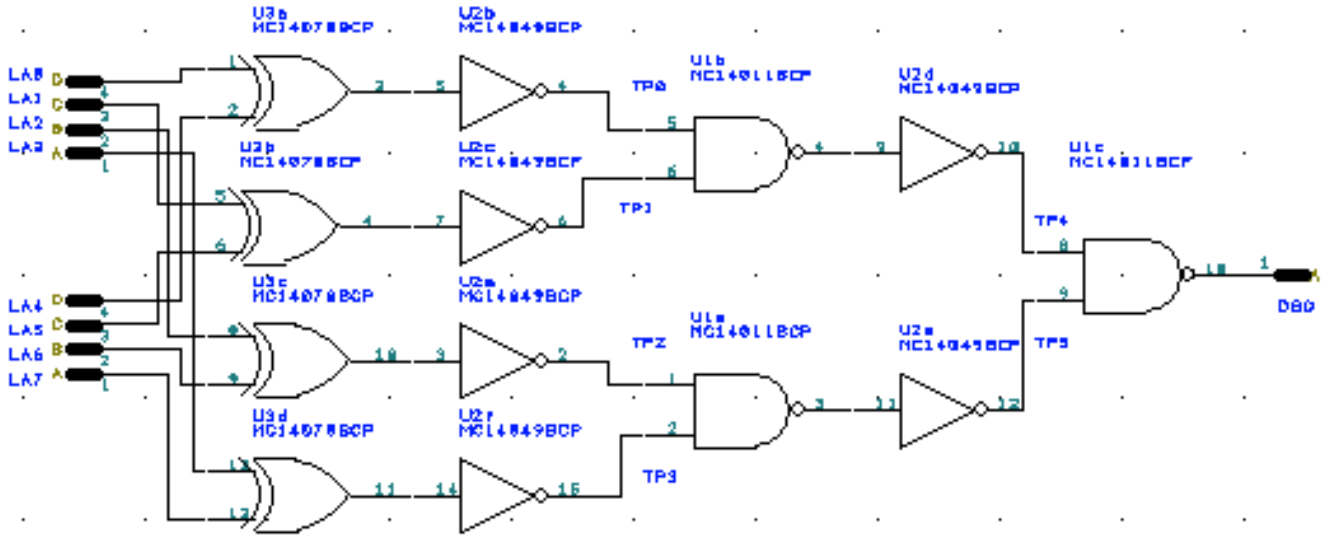
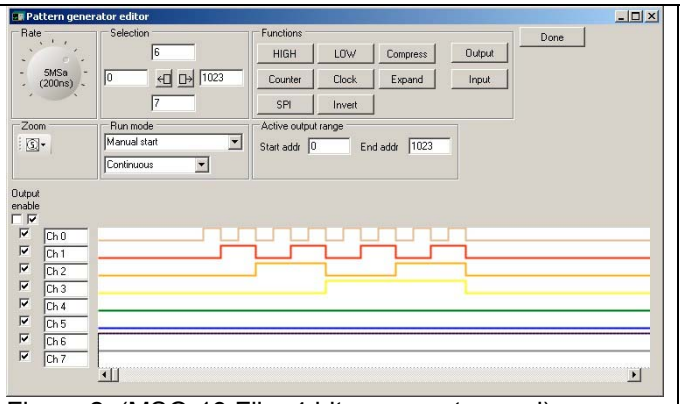
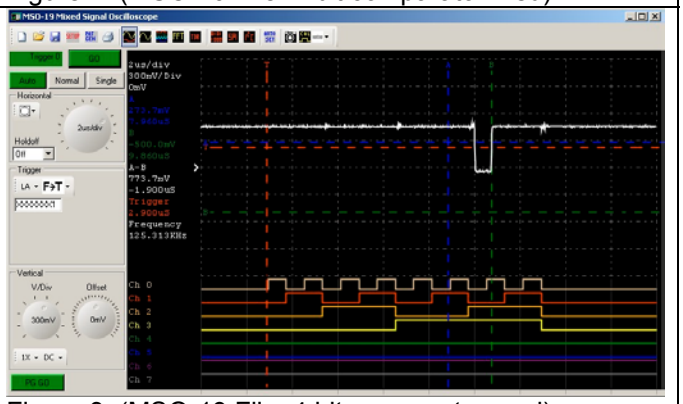


Figure 1:

Binary 4 bit counter on ch0-3 of PG. Steady state level on ch4..7 of PG.	 Figure 2: (MSO-19 File: 4 bit comparator.msd)
The low pulse on the output of the comparator ,shown on the Oscilloscope trace, signifies a match between the mystery code and the counter value. The Mystery code is 1100 and the low pulse shows up just a bit behind the 1100 count. The delay is due to the propagation delay of the circuit.	 Figure 3: (MSO-19 File: 4 bit comparator.msd)

Probing around the circuit we can track the progression of the comparator signal.

TP0

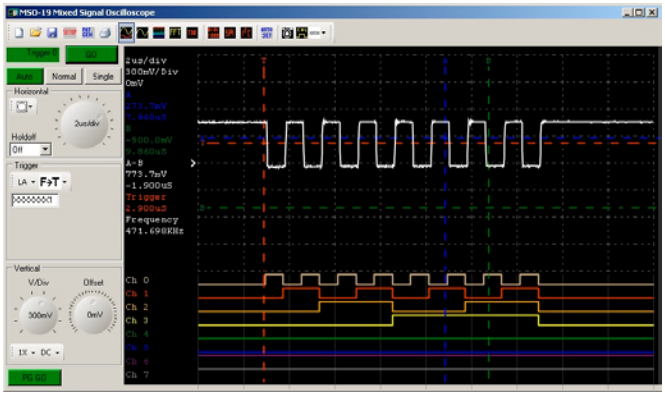


Figure 5: (MSO-19 File: 4 bit comparator TP0.msd)

TP1

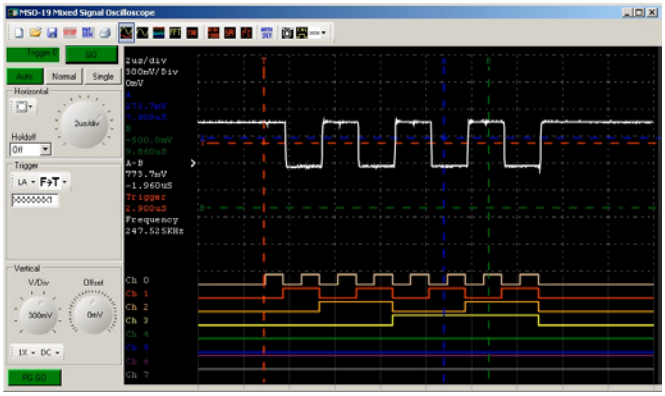


Figure 5: (MSO-19 File: 4 bit comparator TP1.msd)

TP2

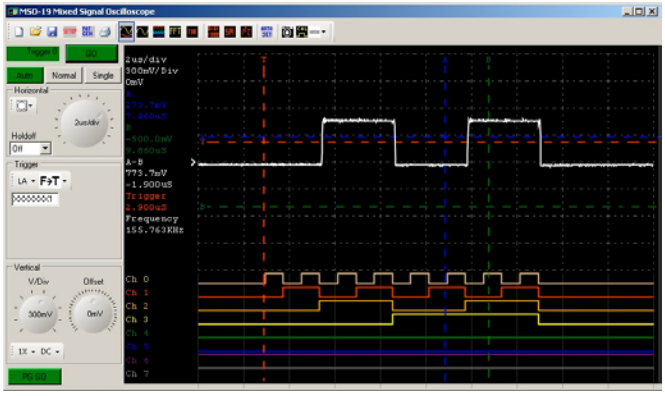


Figure 6: (MSO-19 File: 4 bit comparator TP2.msd)

TP3

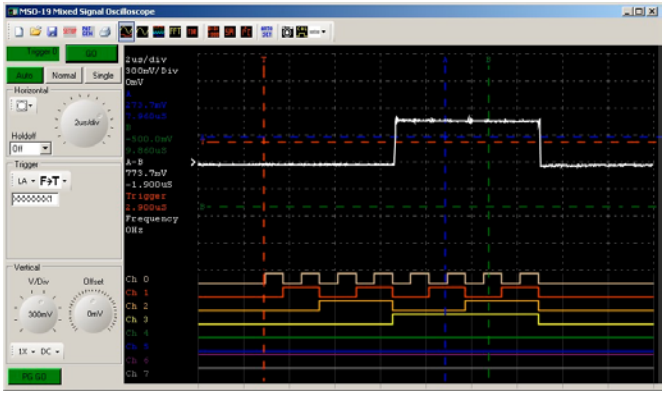


Figure 7: (MSO-19 File: 4 bit comparator TP3.msd)

Halfway outputs are:

TP4

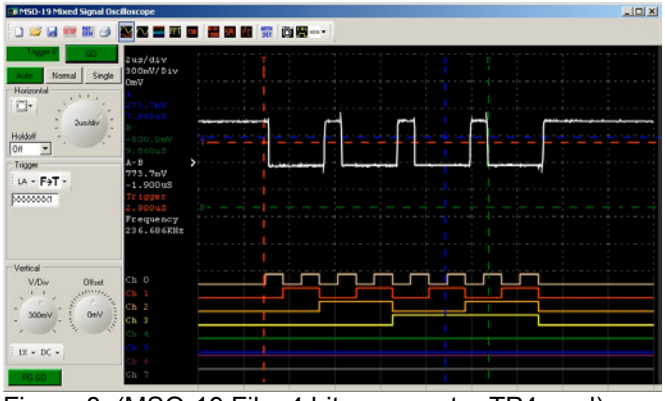


Figure 8: (MSO-19 File: 4 bit comparator TP4.msd)

TP5

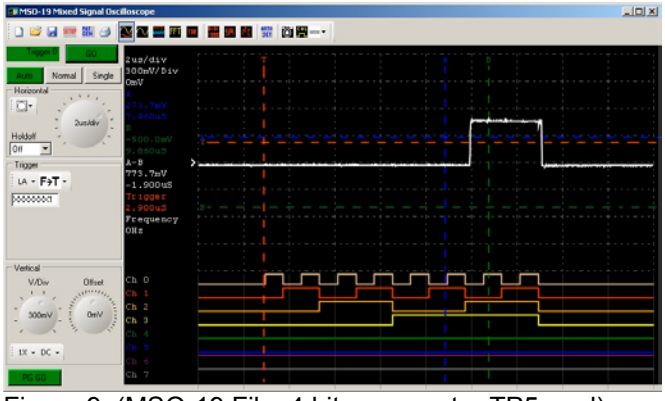
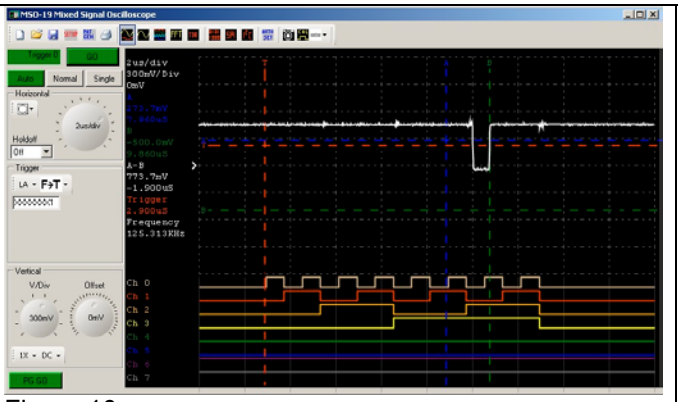


Figure 9: (MSO-19 File: 4 bit comparator TP5.msd)

Combining the TP4 and TP5 waveform we have a single low going pulse at the correct location. The final result is inverted because NAND gate is used in the final stage logic. One can add an Inverter, or use an AND gate to get a positive going pulse.	 Figure 10:

Set-Reset latch

Reference: Radio Shack Electronics Learning Lab (28-280) Workbook 2, page 27.

Tools: Radio Shack Electronics Learning Lab
ICD4001 IC
Link Instruments MSO-19 Oscilloscope/Logic Analyzer/Pattern Generator

Overview: This lab is a supplement to the Radio Shack Electronics Learning Lab. It is also a demonstration of the MSO-19 Logic Analyzer and Pattern Generator.

Memory is another important building block in today's digital circuit. The ability to remember a logic state combined with other fundamental digital logic building blocks form the basis of digital computing. In this exercise, we will examine the function of a simple Set-Reset Latch (SR latch). A SR latch can be constructed from two NOR gates.

The MSO-19 Pattern Generator output pins will replace the two input switches of the original lab. The operation of the circuit will be monitored on the Logic Analyzer pins of the MSO-19.

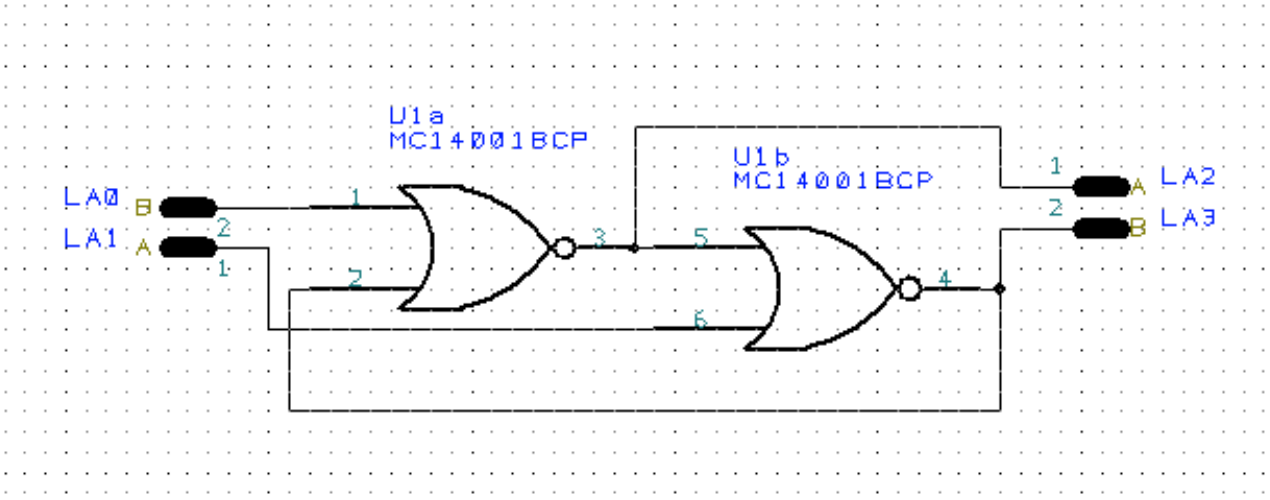


Figure 1:

The pattern generator will provide the Set and Reset signal. We will examine the output on the Logic analyzer channels 0 to 3.

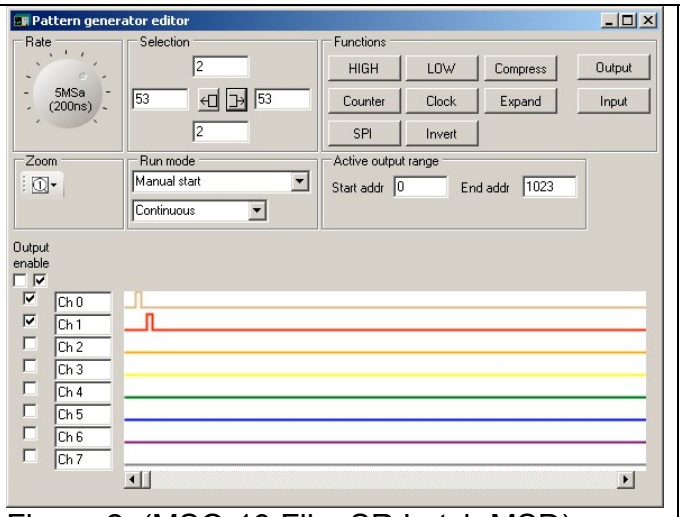


Figure 2: (MSO-19 File: SR Latch.MSD)

Channel 0 shows the “Set” signal.
Channel 1 shows the “Reset” signal.
Channel 2 shows “Q” of the Set-Reset latch
Channel 3 shows “/Q” of the Set-Reset latch.

Toggling the Set and Reset pin, we see the output pins go high and low.

The complementary output pin “/Q” follows the non-inverting output “Q”. The delay between the two outputs is exactly half of the input to output delay of the whole circuit. This is because the signal needs to propagate though two levels of NOR gate.

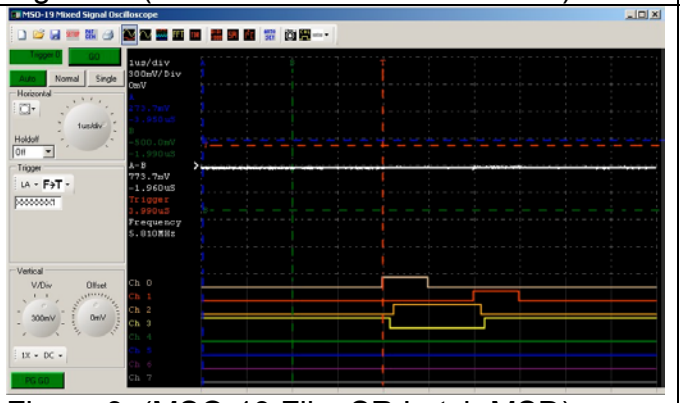


Figure 3: (MSO-19 File: SR Latch.MSD)

Flip-Flops

Reference: Radio Shack Electronics Learning Lab (28-280) Workbook 2, pages 68 and 69.

Tools: Radio Shack Electronics Learning Lab
ICD4013 and ICD4049 ICs
Link Instruments MSO-19 Oscilloscope/Logic Analyzer/Pattern Generator

Overview: This lab is a supplement to the Radio Shack Electronics Learning Lab. It is also a demonstration of the MSO-19 Logic Analyzer and Pattern Generator.

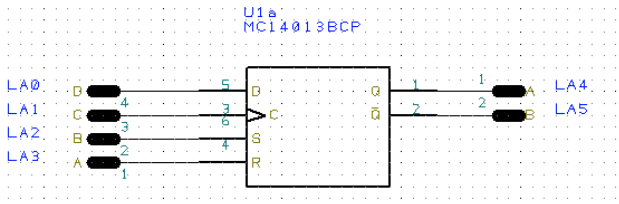
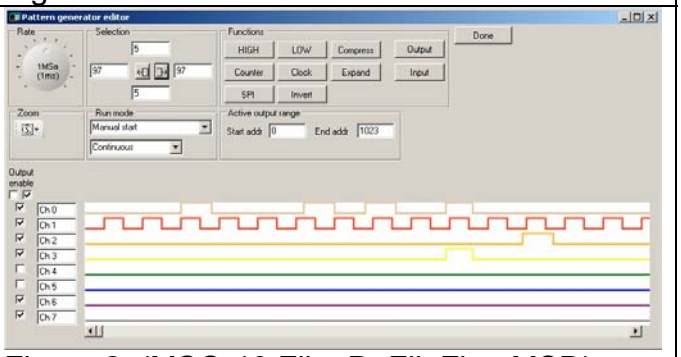
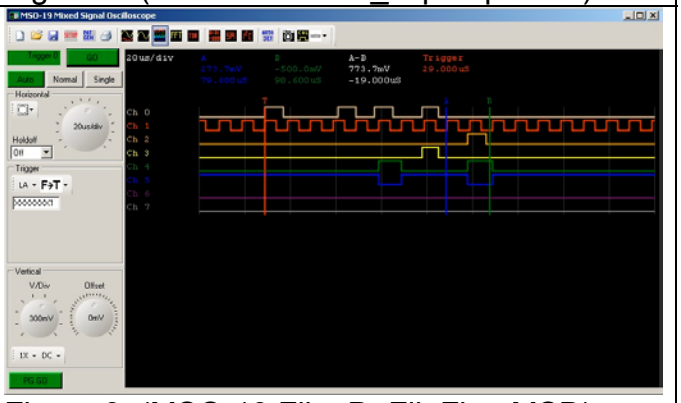
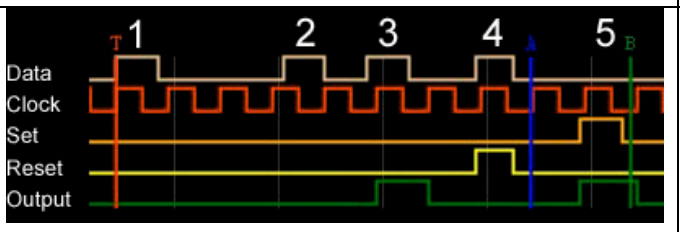
In this exercise we will explore the “D” and “T” flip-flop circuits.

The “D” flip-flop is used as a storage element in a digital circuit. It is a latch with Set-Reset functions and a complementary output. In addition to functioning as a storage element it can also be used in a counter design.

The “T” flip-flop is used in counter and divider designs.

In this exercise we will explore the differences between the two different types of flip-flops.

The MSO-19 Pattern Generator output pins will replace the four input switches of the original lab. The operation of the circuit will be monitored on the Logic Analyzer pins of the MSO-19.

“D” flip-flop	
	 Figure 1:
Configure MSO-19’s Pattern Generator to create the necessary control signals: Data, Clock, Set and Reset. PG Channel 0 is Data PG Channel 1 is Clock PG Channel 2 is Set PG Channel 3 is Reset	 Figure 2: (MSO-19 File: D_FlipFlop.MSD)
LA Channel 0 is Data LA Channel 1 is Clock LA Channel 2 is Set LA Channel 3 is Reset LA Channel 4 is “Q” output LA Channel 5 is “/Q” output The data must be stable for a certain amount of time before the rising clock edge of the receiving circuit. This is called “setup” time. Channel 4 shows the output of the “D” flip-flop. We expected it to follow the Data channel (LA0) and have four pulses. The reason we only see two is a “setup” time error.	 Figure 3: (MSO-19 File: D_FlipFlop.MSD)
This zoomed in view of Figure 3 shows 5 areas of interest. **Area 1:** We don’t see output because there wasn’t enough setup time. **Area 2:** We don’t see output because data went high after the clock edge. **Area 3:** There was enough setup time and we see an output. **Area 4:** We don’t see output because the Reset pin was high. **Area 5:** We have an output even though we don’t have data. This is because the Set pin was high.	

“T” flip-flop method 1

The “T” flip-flop is basically the same as a “D” flip-flop except the Data pin is wired to “/Q”. This forces the data input pin to be the opposite state of the output pin Q. Let’s look at the waveform. We’ll configure the PG again.

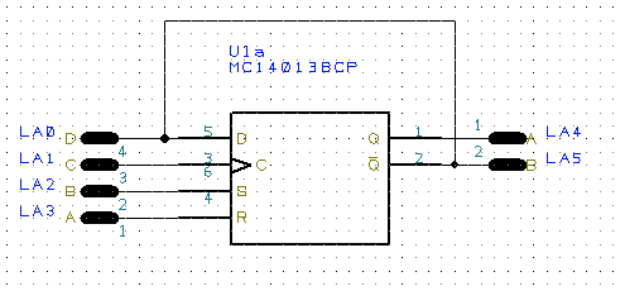


Figure 4:

Configure MSO-19’s Pattern Generator to create the necessary control signals Clock, Set and Reset.

PG Channel 1 is Clock
PG Channel 2 is Set
PG Channel 3 is Reset

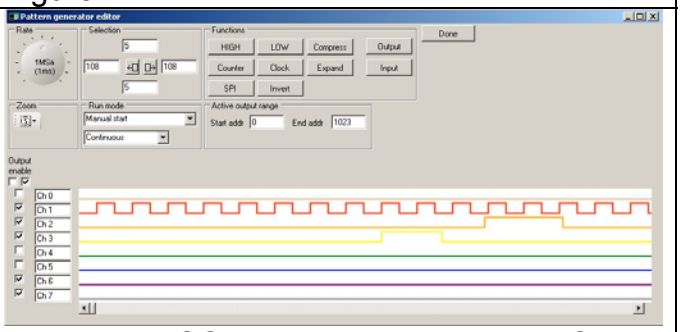


Figure 5: (MSO-19 File: T_FlipFlop_1.MSD)

LA Channel 0 is Data
LA Channel 1 is Clock
LA Channel 2 is Set
LA Channel 3 is Reset
LA Channel 4 is “Q” output
LA Channel 5 is “/Q” output

The “D” pin is now identical to “/Q” pin. SET and RESET still perform the same functions on the “Q” and “/Q” pins

An interesting note, the “Q” pin is now toggling at half the rate of the clock pin. This is a divide by two counter and is the basis for a Binary Counter.

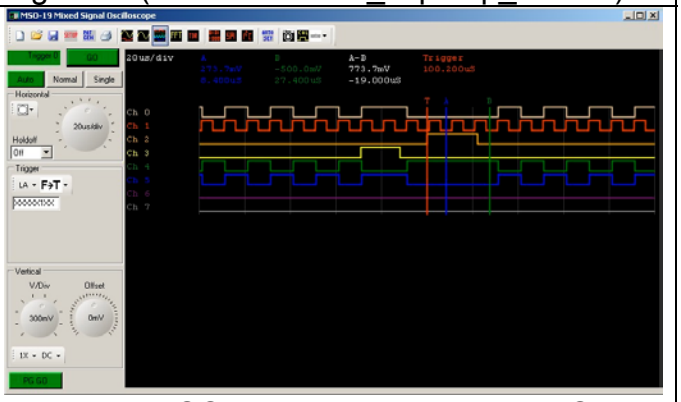


Figure 6: (MSO-19 File: T_FlipFlop_1.MSD)

Another look at the circuit without the SET and RESET signals.

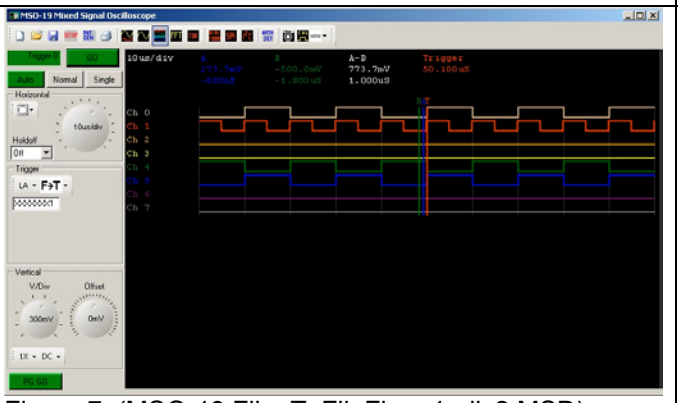


Figure 7: (MSO-19 File: T_FlipFlop_1_div2.MSD)

“T” flip-flop method 2

Another way to create a “T” flip-flop is to put an Inverting Gate after the “Q” signal and feed it back to the “D” pin.

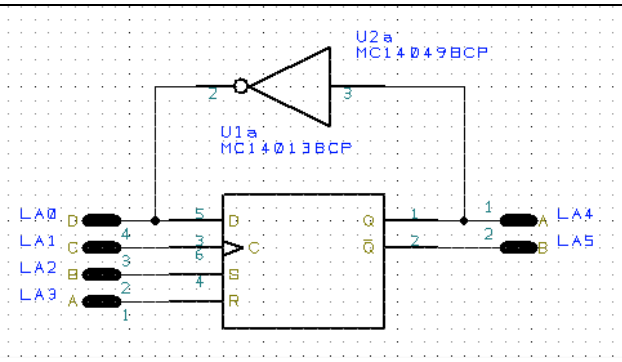


Figure 8:

Both methods perform the same function. The only difference is the extra propagation delay caused by the Inverting Gate and the wiring delay.

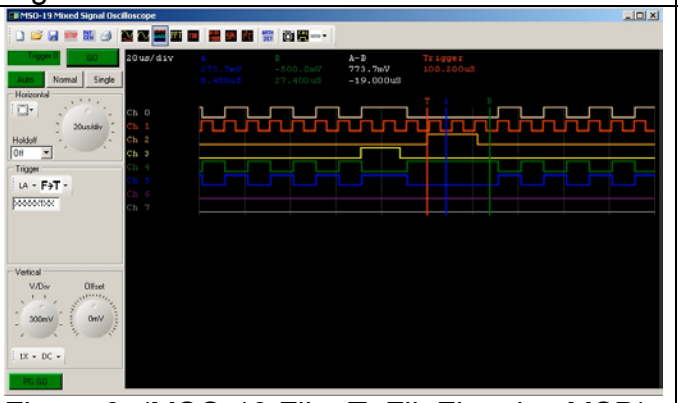


Figure 9: (MSO-19 File: T_FlipFlop_inv.MSD)

In figure 10 we configured the MSO-19 Logic Analyzer to sample at a faster rate and we zoomed in. This gave us a much more detailed view of the point of interest.

The lag caused by the Inverting gate can be measured by looking at the point that “Q” goes low and “D” goes high. We have placed the Logic Analyzer cursors “B” and “A” on those points. We can use the cursor measurement on the top of screen to see the time delay as “20nS”,

Figure 10: (MSO-19 File: FlipFlop_inv_closeup.MSD)

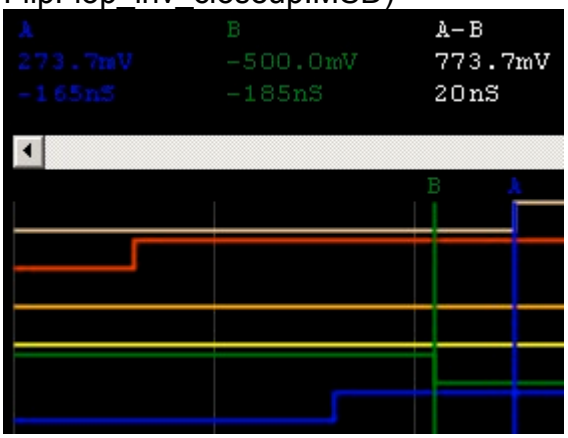


Figure 10a:

Counters

Reference: Radio Shack Electronics Learning Lab (28-280) Workbook 2, pages 72, 73, 12 and 13.

Tools: Radio Shack Electronics Learning Lab
CD4001, CD4013, CD 4017, CD 4029 and CD4070 ICs
Link Instruments MSO-19 Oscilloscope/Logic Analyzer/Pattern Generator

Overview: This lab is a supplement to the Radio Shack Electronics Learning Lab. It is also a demonstration of the MSO-19 Logic Analyzer and Pattern Generator.

In this exercise we will explore 4 types of counters: Ripple, Synchronous, Decade and Binary.

In the previous exercise we learned how “D” and “T” flip-flops operate. The toggling action forms the foundation of counters. Large counters can be built by combining multiple flip-flops.

The MSO-19 Pattern Generator output pins will replace the input switches of the original lab. The operation of the circuit will be monitored on the Logic Analyzer pins of the MSO-19.

2 bit ripple counter

The ripple counter is simple to construct. The count will increment with each clock pulse and will reset when the reset pin is active.

"/Q" from the previous stage is used as a clock for the next stage. Since the clock signal ripples down the counter chain the outputs do not switch simultaneously.

As the clock speed and counter size increase glitches of false count will occur. This is due to asynchronous output switching.

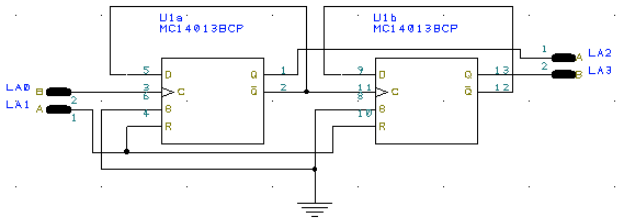


Figure 1:

The MSO-19 Pattern Generator will provide a clock and a reset pulse.

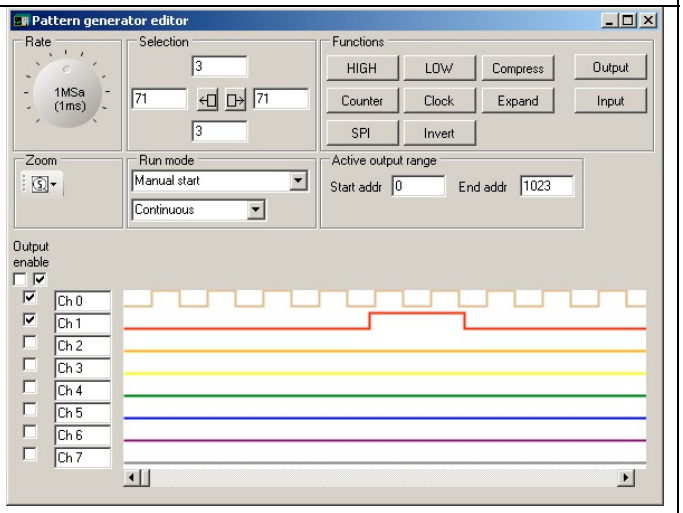


Figure 2:
(MSO-19 File: 2 bit counter ripple.MSD)

LA Channel 0: Clock
LA Channel 1: Reset
LA Channel 2: Q0
LA Channel 3: Q1

The count starts when the reset signal goes inactive. You will see the binary count cycling between 00, 01, 10,11, 00, 01, 10, 11… on pins Q0 and Q1

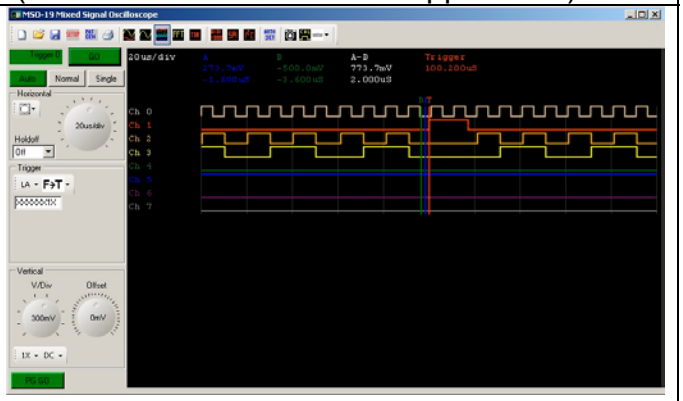


Figure 3:
(MSO-19 File: 2 bit counter ripple.MSD)

In figure 4 we increased the sampling rate of the MSO-19 Logic Analyzer to show the asynchronous characteristics of the circuit.

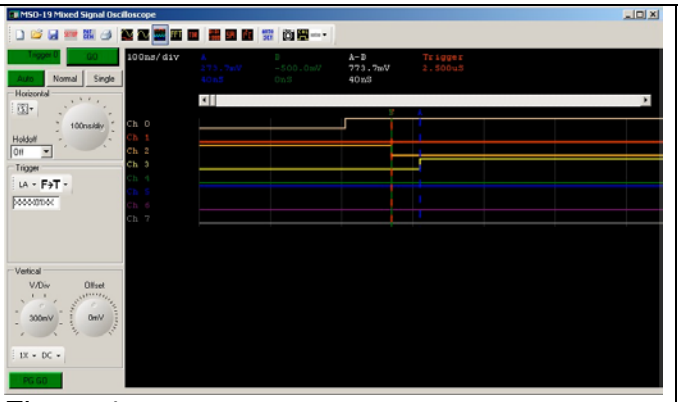


Figure 4:
(MSO-19 File: 2 bit counter ripple_closeup.MSD)

A closer look shows that Q0 and Q1 do not transition at the same time. They are about 40nS apart.
If you look at the Logic Analyzer Statelist window you will see the count on pins 2 and 3 going from “01” to ”00” to ”10” instead of “01” to ”10”. The “00” was a false count.

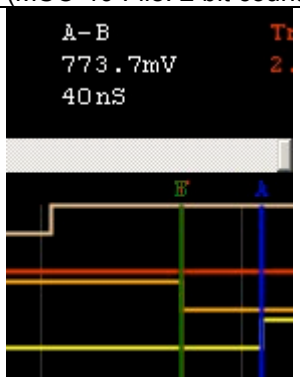


Figure 4A:

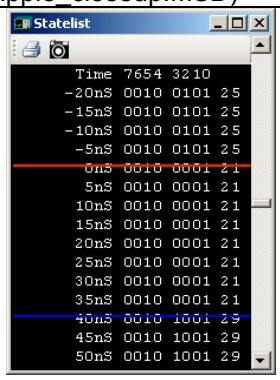


Figure 4B:

Figure 5 shows what happens when you run the clock at too fast a rate. If the propagation delay exceeds the clock rate the counter stops working properly.

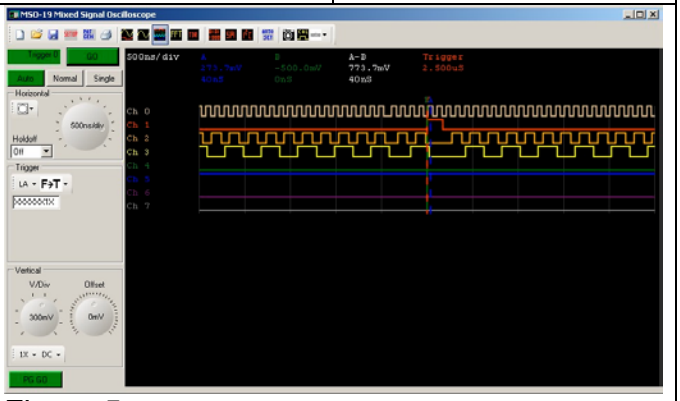


Figure 5:
(MSO-19 File: 2 bit counter ripple 100M clk.MSD)

2 bit synchronous counter

With the synchronous counter all the flip-flops change state on the same clock edge. The “D in” for each flip-flop stage is generated with external logic gates. This kind of counter can operate at a higher speed. The large amount of external logic is a disadvantage. The top speed is limited by the propagation delay of the feedback logic.

An extra XOR gate is required in the second stage to make the input toggle. The same clock is shared between both flip-flops.

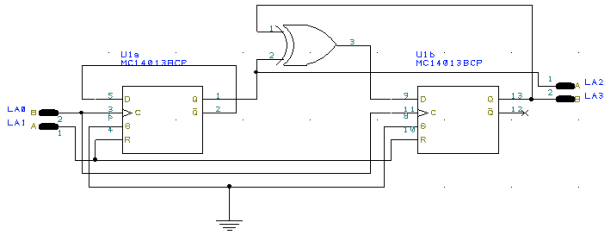


Figure 6:

LA Channel 0: Clock
LA Channel 1: Reset
LA Channel 2: Q0
LA Channel 3: Q1

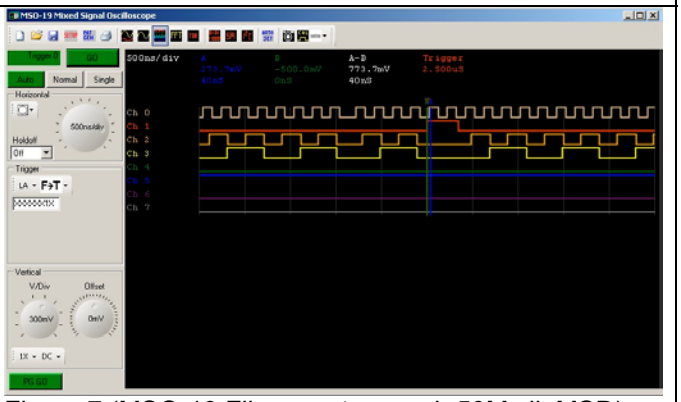


Figure 7:(MSO-19 File: counter synch 50M clk.MSD)

Figures 7A and 7B show how Q0 and Q1 are synchronized.

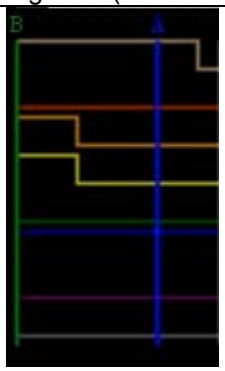


Figure 7A:

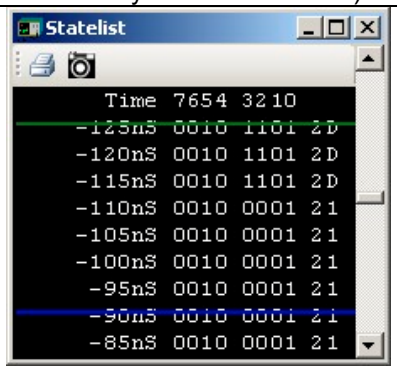


Figure 7B:

Figure 8 shows what happens when the sample clock is shorter than the propagation delay of the external logic gates.

At input frequency of 50Mhz the counter works fine. But at 100Mhz, the second stage can not get its Din from the XOR in time, and the output Q1 failed to count correctly.

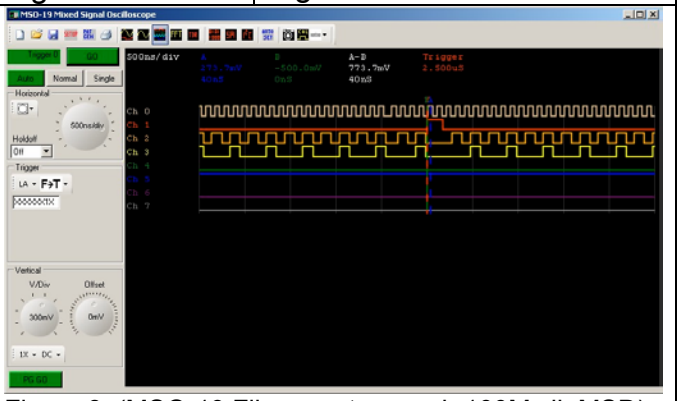


Figure 8: (MSO-19 File: counter synch 100M clk.MSD)

2 bit synchronous counter 1 of 4 decoder

In this decoder the 4 possible states of the 2 bit counter are translated into 4 unique status signals. These signals can be used to drive other circuits.

The output of the binary counter is decoded with NOR gates. Refer to page 73 for more details.

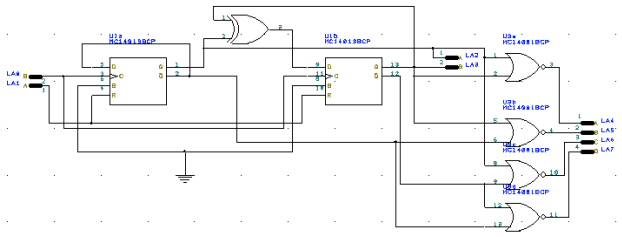


Figure 9:

LA Channel 0: Clock
LA Channel 1: Reset
LA Channel 2: Q0
LA Channel 3: Q1
LA Channel 4: S0
LA Channel 5: S1
LA Channel 6: S2
LA Channel 7: S3

Q0 and Q1 are the outputs of the counter. S0, S1, S2 and S3 are the decoded translations of Q0 and Q1.

When Q0=0 and Q1=0 S0 =1
When Q0=1 and Q1=0 S1 =1
When Q0=0 and Q1=1 S2 =1
When Q0=1 and Q1=1 S3 =1

Since we used a synchronous counter there were no errors in our decoder output. Had we used a ripple counter we would have seen narrow glitches due to the asynchronous nature of the counter.

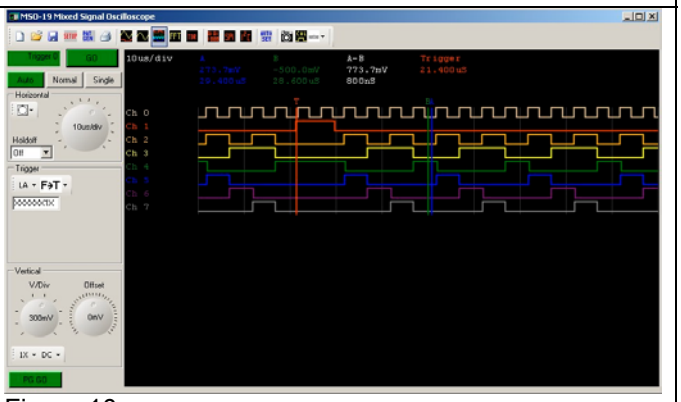


Figure 10:
(MSO-19 File: counter synch 2M clk 1of4 seq.MSD)

Decade counter

We can buy larger counters in single chip packages. This saves time and space.

A decade counter is a larger version of the circuit we just built. It counts to 10. The CD4017 is both a decade counter and a decoder in one package (see page 12).

Again, we will control it using the MS0-19 PG pins.

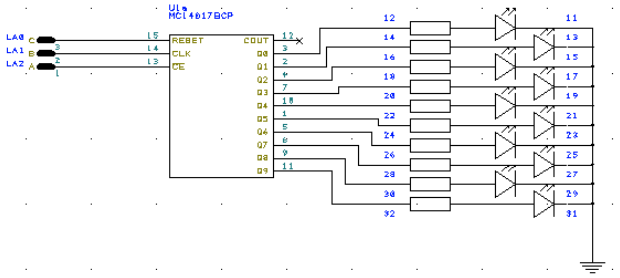


Figure 11:

The MSO-19 Pattern Generator will provide Reset, Clock, and Count Enable.

PG Channel 0: Reset
PG Channel 1: Clock
PG Channel 2: /CE

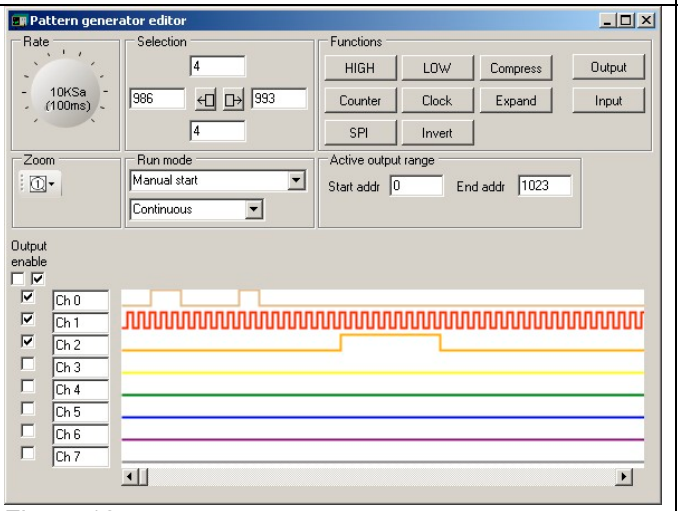


Figure 12:
(MSO-19 File: Decade Counter Decoder.MSD)

LA Channel 0: Reset
LA Channel 1: Clock
LA Channel 2: /CE
LA Channel 3: S0
LA Channel 4: S1
LA Channel 5: S2
LA Channel 6: S3
LA Channel 7: Carry out

You will notice that S0, S1, S2 and S3 appear the same as they did the previous example.

Reset will clear the count.

When /CE is high the count stops.

The Carry out is used to cascade to the signal into additional counter chips.

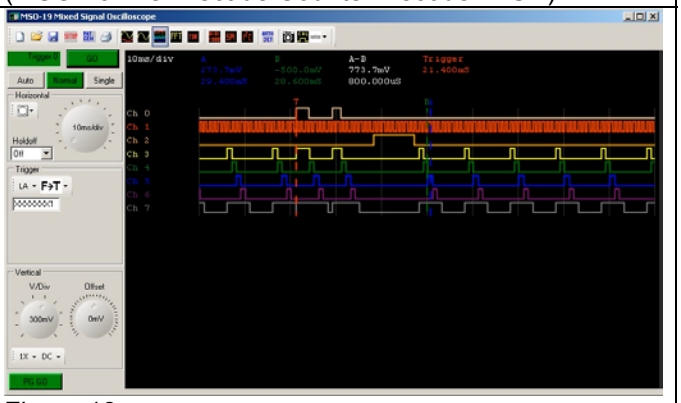


Figure 13:
(MSO-19 File: Decade Counter Decoder.MSD)

Binary Up/Down counter

The CD4029 is an up/down binary/decade loadable counter (see page 13).

An up/down counter can increment or decrement the count.

A decade counter goes from 0 to 9 and repeats.

A binary counter goes from 0 to 15 and repeats.

A loadable counter allows you to start the count at a specific value instead of always starting at 0.

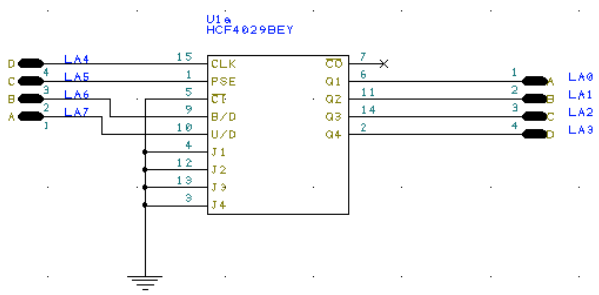


Figure 14:

We will use the MSO-19 Pattern Generator to exercise the various control pins.

PG Channel 4: Clock
PG Channel 5: PSE
PG Channel 6: Binary/Decade
PG Channel 7: Up/Down

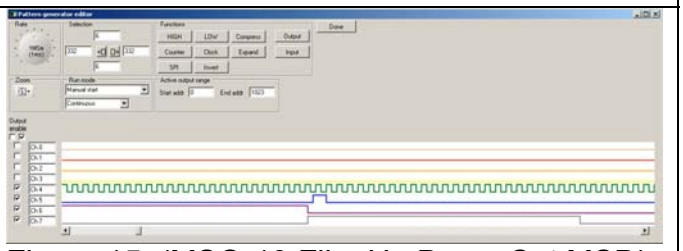


Figure 15: (MSO-19 File: Up Down Cnt.MSD)

LA Channel 0: Q0
LA Channel 1: Q1
LA Channel 2: Q2
LA Channel 3: Q3
LA Channel 4: Clock
LA Channel 5: PSE
LA Channel 6: Binary/Decade
LA Channel 7: Up/Down

Since there is no Reset pin on the CD4029, we pre-wire the parallel load data pins to 0000. When PSE (parallel load enable) is active we will clock in 0000, which is the same as Reset.

Channel 6 is Binary or Decade mode.
As you can see the first half of the buffer is Binary mode and second half is Decade mode.

Channel 7 selects up or down count.
The first half of each section is high and the second is low.

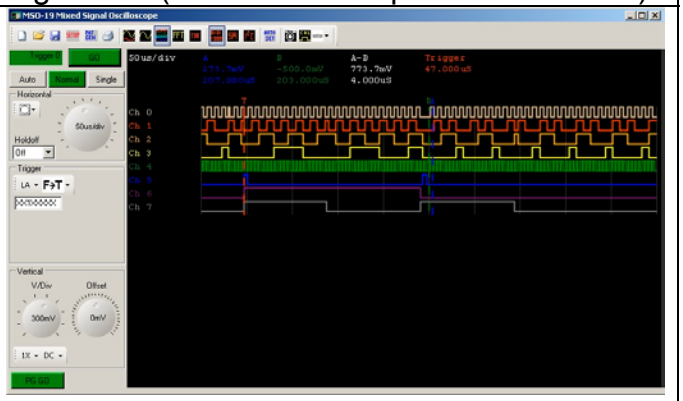
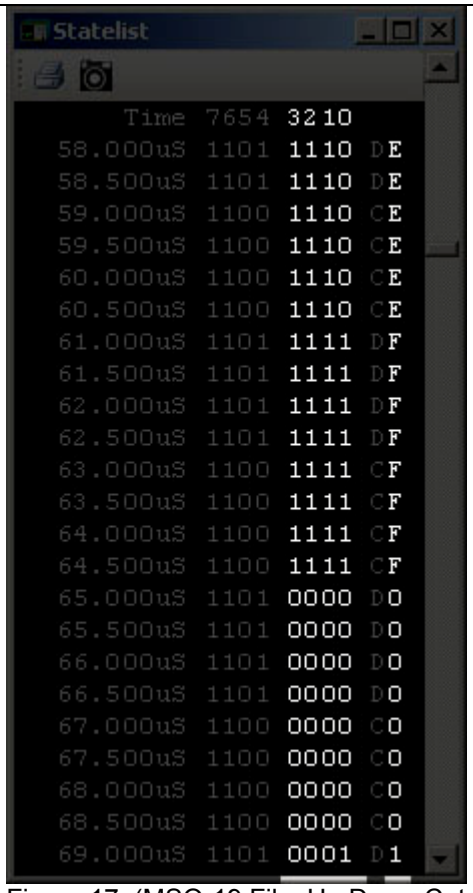
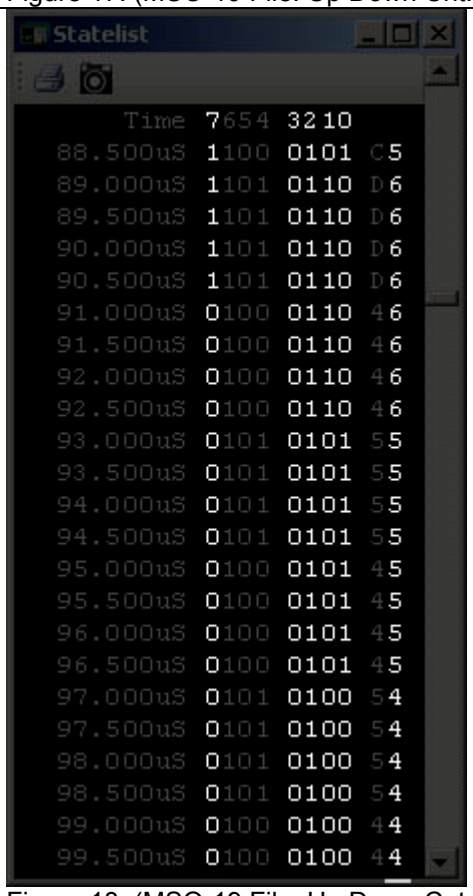
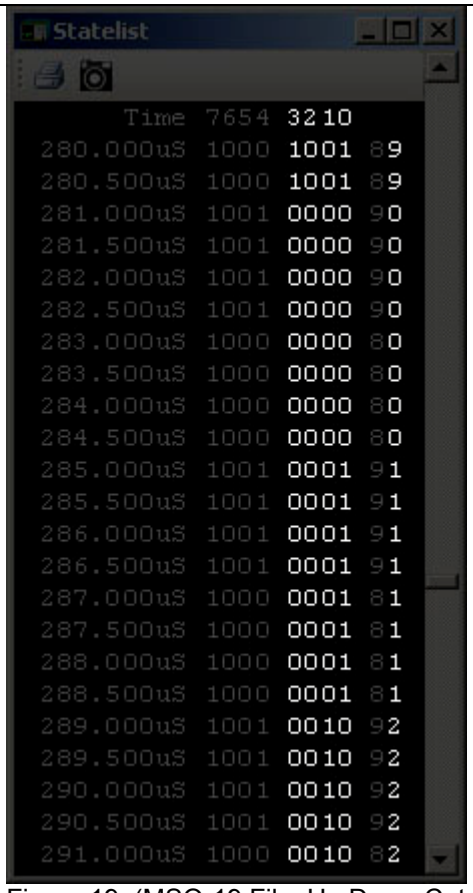
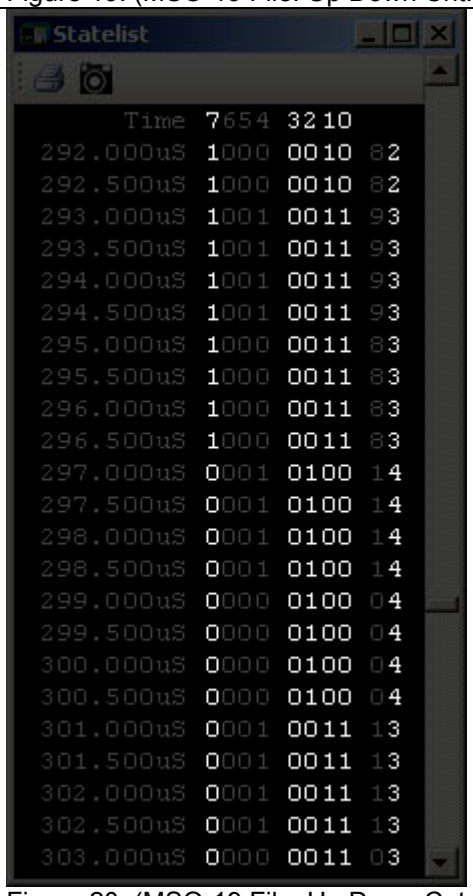


Figure 16: (MSO-19 File: Up Down Cnt.MSD)

Examining the lower nibble of Statelist output will show the count sequence. Binary Up count	 Figure 17: (MSO-19 File: Up Down Cnt.MSD)
Binary Count down selected, count is going down. Bit 7 (U/D) going from 1 to 0.	 Figure 18: (MSO-19 File: Up Down Cnt.MSD)

Decade count up. The lower nibble only counts up to 9, then it wraps around to 0.	 Figure 19: (MSO-19 File: Up Down Cnt.MSD)
Decade count down selected, notice the lower nibble counts from 2 to 4 back down to 3 as the bit7(U/D) went to 0 to select counting down.	 Figure 20: (MSO-19 File: Up Down Cnt.MSD)